S905X2 REF BOARD DIAGRAM

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00- Power tree
01- Power
02- CPU I/O
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05- Ethernet
06- USB & PCIe
07- SDIO WIFI
08- Audio & CVBS
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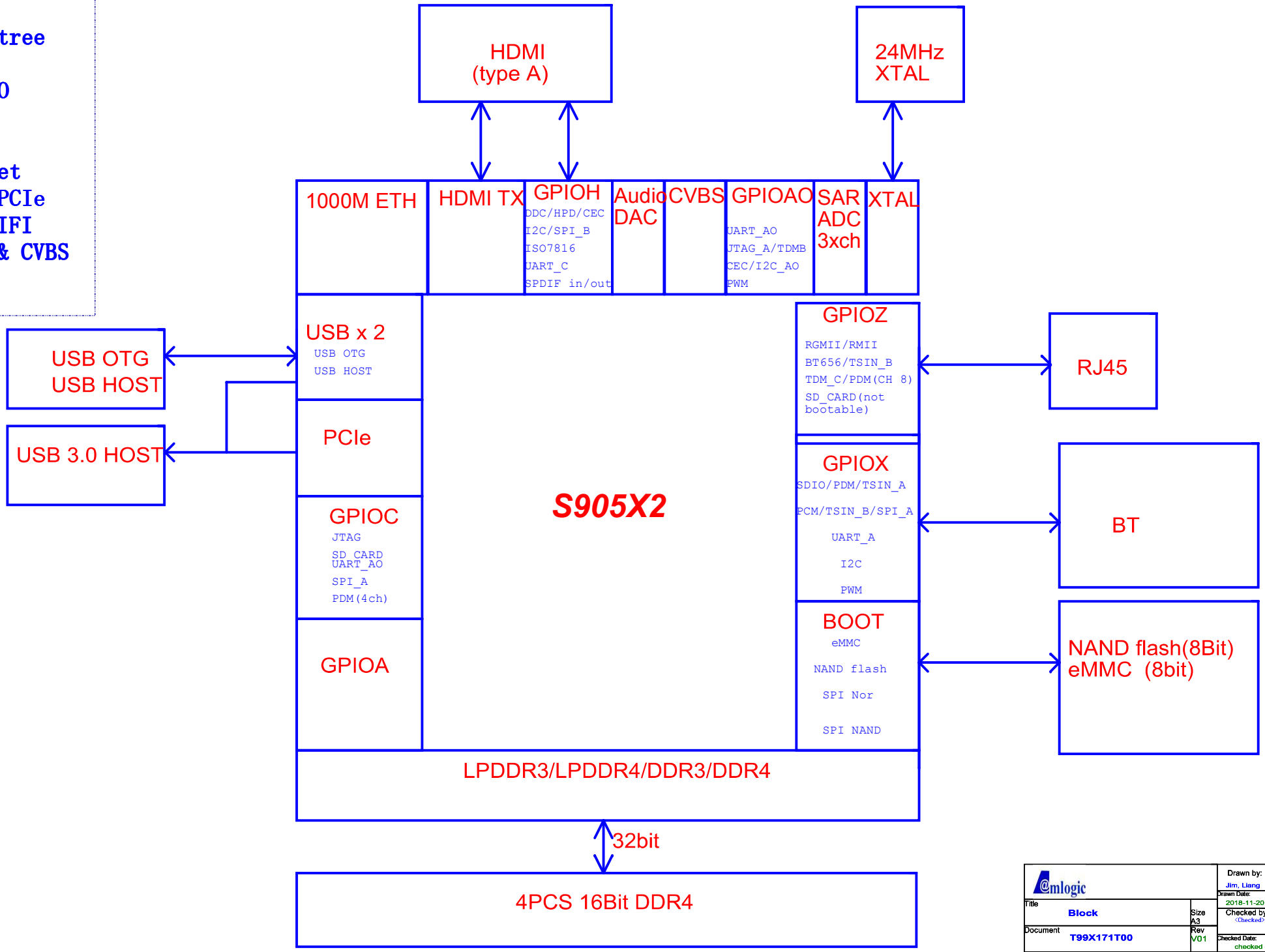
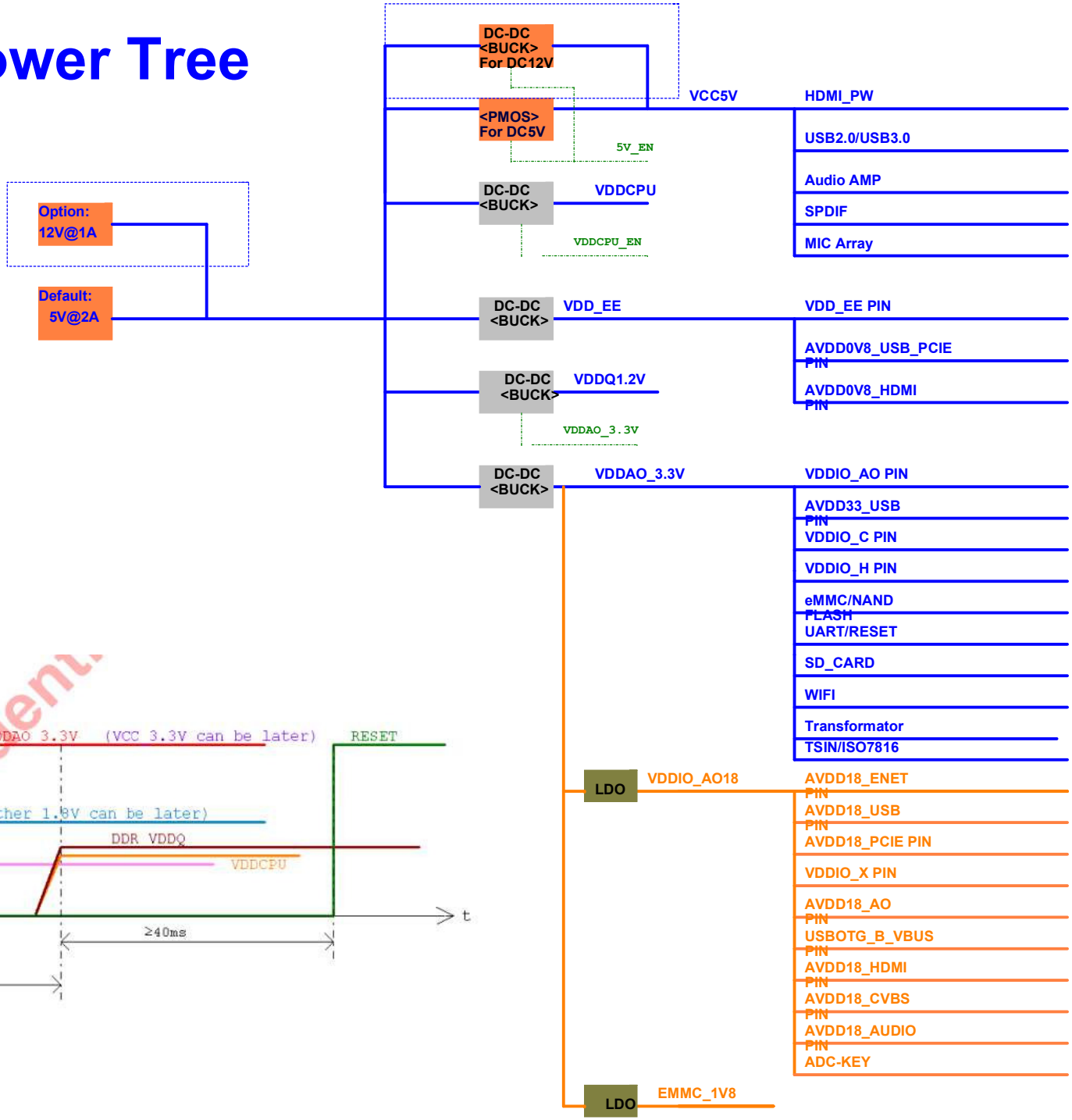
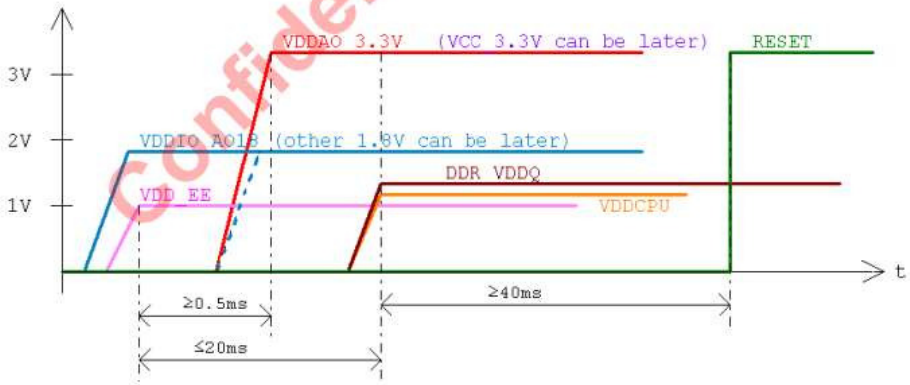


Amlogic		Drawn by: Jim, Liang
Title: Block	Size: A3	Drawn Date: 2018-11-20
Document: T99X171T00	Rev: V01	Checked by: <Checked>
Date: Monday, December 27, 2021	Sheet 1 of 15	Checked Date: checked date

Power Tree

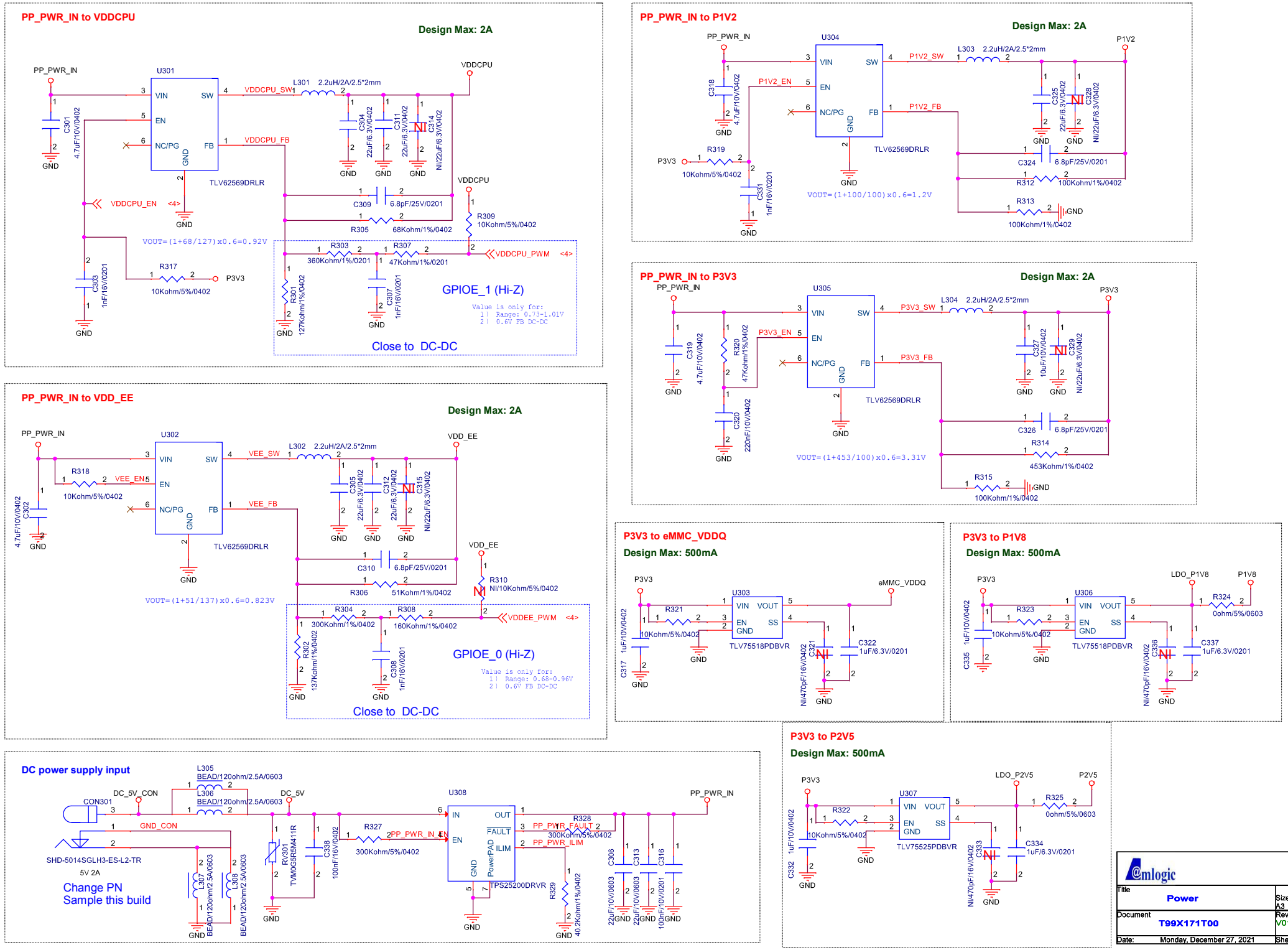


Example power on sequence:



Confidential

Amlogic			Drawn by: Jim, Liang
Title: Power tree	Size: A3		Drawn Date: 2018-11-20
Document: T99X171T00	Rev: V01		Checked by: <Checked>
Date: Monday, December 27, 2021	Sheet 2 of 15		Checked Date: checked date


PP_PWR_IN to VDDCPU
Design Max: 2A
PP_PWR_IN
U301
VIN
SW
EN
NC/PG
FB
GND
TLV62569DRLR
VDDCPU_SW
L301 2.2uH/2A/2.5*2mm
VDDCPU
VDDCPU_FB
C301 4.7uF/10V/0402
C304 22uF/6.3V/0402
C311 22uF/6.3V/0402
C314 NI/22uF/6.3V/0402
VDDCPU_EN <4>
C309 6.8pF/25V/0201
R305 68Kohm/1%/0402
R309 10Kohm/5%/0402
VOUT=(1+68/127)x0.6=0.92V
R303 360Kohm/1%/0201
R307 47Kohm/1%/0201
VDDCPU_PWM <4>
R317 10Kohm/5%/0402
P3V3
C303 1nF/16V/0201
R301 127Kohm/1%/0402
C307 1nF/16V/0201
GPIOE_1 (Hi-Z)
Value is only for:
1) Range: 0.73-1.01V
2) 0.6V FB DC-DC
Close to DC-DC
PP_PWR_IN to P1V2
Design Max: 2A
U304
P1V2_SW
L303 2.2uH/2A/2.5*2mm
P1V2
P1V2_EN
P1V2_FB
C318 4.7uF/10V/0402
C325 22uF/6.3V/0402
C328 NI/22uF/6.3V/0402
R319 10Kohm/5%/0402
C331 1nF/16V/0201
C324 6.8pF/25V/0201
R312 100Kohm/1%/0402
R313 100Kohm/1%/0402
VOUT=(1+100/100)x0.6=1.2V
PP_PWR_IN to P3V3
Design Max: 2A
U305
P3V3_SW
L304 2.2uH/2A/2.5*2mm
P3V3
P3V3_EN
P3V3_FB
C319 4.7uF/10V/0402
R320 47Kohm/1%/0402
C320 220nF/10V/0402
C327 10uF/10V/0402
C329 NI/22uF/6.3V/0402
C326 6.8pF/25V/0201
R314 453Kohm/1%/0402
R315 100Kohm/1%/0402
VOUT=(1+453/100)x0.6=3.31V
PP_PWR_IN to VDD_EE
Design Max: 2A
U302
VEE_SW
L302 2.2uH/2A/2.5*2mm
VDD_EE
R318 10Kohm/5%/0402
VEE_EN
VEE_FB
C302 4.7uF/10V/0402
C305 22uF/6.3V/0402
C312 22uF/6.3V/0402
C315 NI/22uF/6.3V/0402
C310 6.8pF/25V/0201
R306 51Kohm/1%/0402
R310 NI/10Kohm/5%/0402
VOUT=(1+51/137)x0.6=0.823V
R304 300Kohm/1%/0402
R308 160Kohm/1%/0402
VDDEE_PWM <4>
R302 137Kohm/1%/0402
C308 1nF/16V/0201
GPIOE_0 (Hi-Z)
Value is only for:
1) Range: 0.68-0.96V
2) 0.6V FB DC-DC
Close to DC-DC
P3V3 to eMMC_VDDQ
Design Max: 500mA
U303
VIN
VOUT
EN
SS
GND
TLV75518PDBVR
eMMC_VDDQ
R321 10Kohm/5%/0402
C317 1uF/10V/0402
C321 NI/470pF/16V/0402
C322 1uF/6.3V/0201
P3V3 to P1V8
Design Max: 500mA
U306
LDO_P1V8
P1V8
R323 10Kohm/5%/0402
R324 0ohm/5%/0603
C335 1uF/10V/0402
C336 NI/470pF/16V/0402
C337 1uF/6.3V/0201
DC power supply input
L305 BEAD/120ohm/2.5A/0603
L306 BEAD/120ohm/2.5A/0603
DC_5V_CON
DC_5V
CON301
GND_CON
SHD-5014SGLH3-ES-L2-TR
5V 2A
Change PN
Sample this build
L307 BEAD/120ohm/2.5A/0603
L308 BEAD/120ohm/2.5A/0603
RV301 TVM0G5R5M411R
C338 100nF/16V/0402
R327 300Kohm/5%/0402
U308
IN
OUT
EN
FAULT
ILIM
GND
PowerPAD
TPS25200DRVR
PP_PWR_IN_EN
PP_PWR_FAULT
PP_PWR_ILIM
R328 300Kohm/5%/0402
R329 40.2Kohm/1%/0402
C306 22uF/10V/0603
C313 22uF/10V/0603
C316 100nF/10V/0201
P3V3 to P2V5
Design Max: 500mA
U307
LDO_P2V5
P2V5
R322 10Kohm/5%/0402
R325 0ohm/5%/0603
C332 1uF/10V/0402
C333 NI/470pF/16V/0402
C334 1uF/6.3V/0201
TLV75525PDBVR
amlogic
Drawn by: Jim, Liang
Drawn Date: 2018-11-20
Checked by: <Checked>
Checked Date: checked date
Title: Power
Size: A3
Document: T99X171T00
Rev: V01
Date: Monday, December 27, 2021
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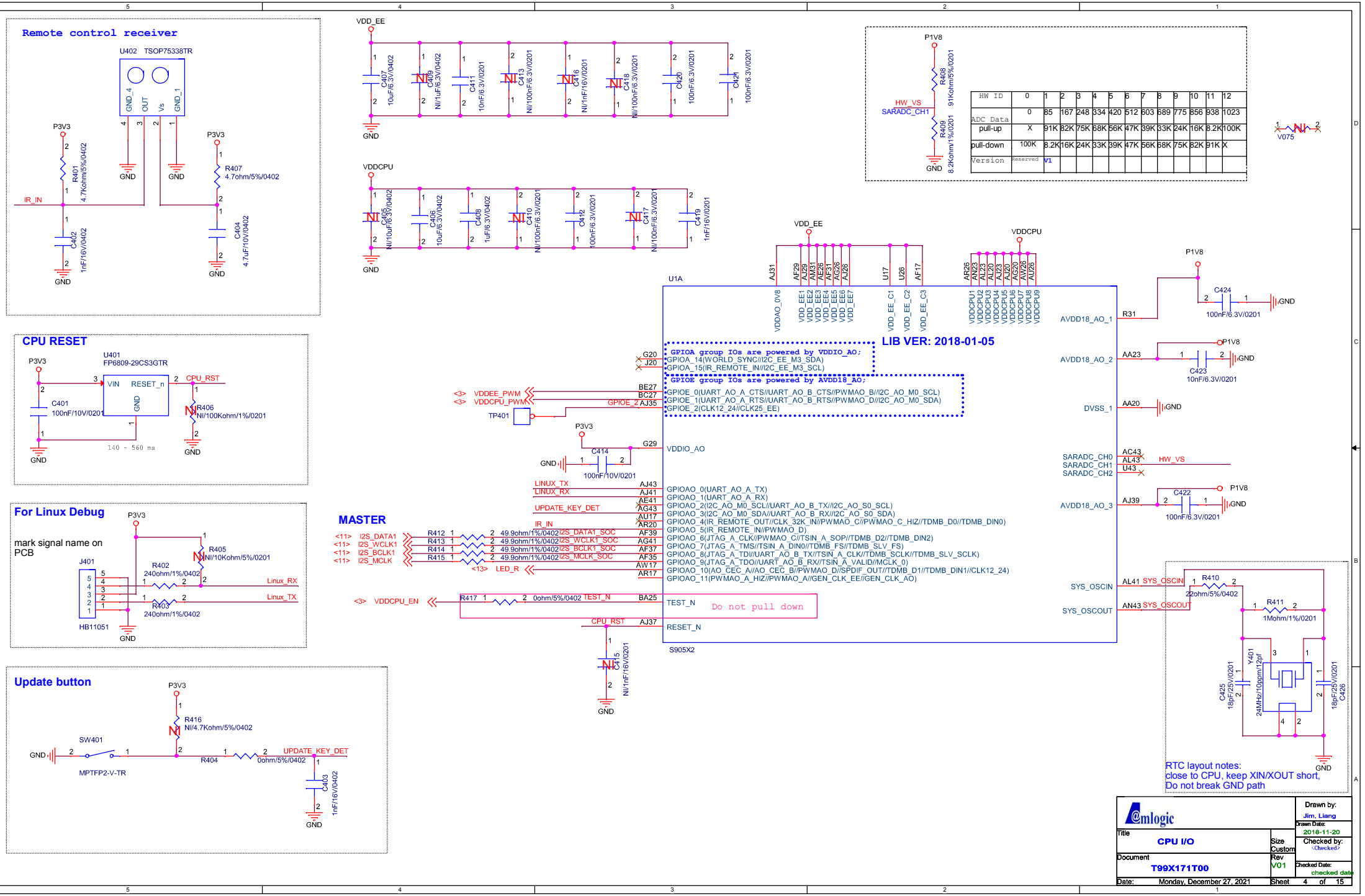
Remote control receiver
U402 TSOP75338TR
GND_4
OUT
Vs
GND_1
P3V3
R401 4.7Kohm/5%/0402
IR_IN
C402 1nF/16V/0402
R407 4.7ohm/5%/0402
C404 4.7uF/10V/0402
GND
CPU RESET
U401 FP6809-29CS3GTR
VIN
RESET_n
CPU_RST
C401 100nF/10V/0201
R406 NI/100Kohm/1%/0201
140 ~ 560 ms
For Linux Debug
mark signal name on PCB
J401
HB11051
R402 240ohm/1%/0402
R403 240ohm/1%/0402
R405 NI/10Kohm/5%/0201
Linux_RX
Linux_TX
Update button
SW401
MPTFP2-V-TR
R416 NI/4.7Kohm/5%/0402
R404 0ohm/5%/0402
UPDATE_KEY_DET
C403 1nF/16V/0402
VDD_EE
C407 10uF/6.3V/0402
C409 NI/1uF/6.3V/0402
C411 10nF/6.3V/0201
C413 NI/100nF/6.3V/0201
C416 NI/1nF/16V/0201
C418 NI/100nF/6.3V/0201
C420 100nF/6.3V/0201
C421 100nF/6.3V/0201
VDDCPU
C405 NI/10uF/6.3V/0402
C406 10uF/6.3V/0402
C408 1uF/6.3V/0402
C410 NI/100nF/6.3V/0201
C412 100nF/6.3V/0201
C417 NI/100nF/6.3V/0201
C419 1nF/16V/0201
P1V8
R408 91Kohm/5%/0201
R409 8.2Kohm/1%/0201
HW_VS
SARADC_CH1
HW ID | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12
ADC Data | 0 | 85 | 167 | 248 | 334 | 420 | 512 | 603 | 689 | 775 | 856 | 938 | 1023
pull-up | X | 91K | 82K | 75K | 68K | 56K | 47K | 39K | 33K | 24K | 16K | 8.2K | 100K
pull-down | 100K | 8.2K | 16K | 24K | 33K | 39K | 47K | 56K | 68K | 75K | 82K | 91K | X
Version | Reserved | V1
V075
U1A
S905X2
LIB VER: 2018-01-05
GPIOA group IOs are powered by VDDIO_AO;
GPIOA_14(WORLD_SYNC//I2C_EE_M3_SDA)
GPIOA_15(IR_REMOTE_IN//I2C_EE_M3_SCL)
GPIOE group IOs are powered by AVDD18_AO;
GPIOE_0(UART_AO_A_CTS//UART_AO_B_CTS//PWMAO_B//I2C_AO_M0_SCL)
GPIOE_1(UART_AO_A_RTS//UART_AO_B_RTS//PWMAO_D//I2C_AO_M0_SDA)
GPIOE_2(CLK12_24//CLK25_EE)
VDDEE_PWM
VDDCPU_PWM
TP401
VDDIO_AO
C414 100nF/10V/0201
LINUX_TX
LINUX_RX
UPDATE_KEY_DET
IR_IN
I2S_DATA1
I2S_WCLK1
I2S_BCLK1
I2S_MCLK
LED_R
VDDCPU_EN
R417 0ohm/5%/0402
TEST_N
Do not pull down
CPU_RST
RESET_N
C415 NI/1nF/16V/0201
AVDD18_AO_1
AVDD18_AO_2
DVSS_1
SARADC_CH0
SARADC_CH1
SARADC_CH2
AVDD18_AO_3
SYS_OSCIN
SYS_OSCOUT
R31
C424 100nF/6.3V/0201
C423 10nF/6.3V/0201
C422 100nF/6.3V/0201
R410 22ohm/5%/0402
R411 1Mohm/1%/0201
Y401 24MHz/10ppm/12pf
C425 18pF/25V/0201
C426 18pF/25V/0201
RTC layout notes:
close to CPU, keep XIN/XOUT short,
Do not break GND path
Amlogic
Title
CPU I/O
Size Custom
Document
T99X171T00
Rev V01
Drawn by: Jim, Liang
Drawn Date: 2018-11-20
Checked by: <Checked>
Checked Date: checked date
Date: Monday, December 27, 2021
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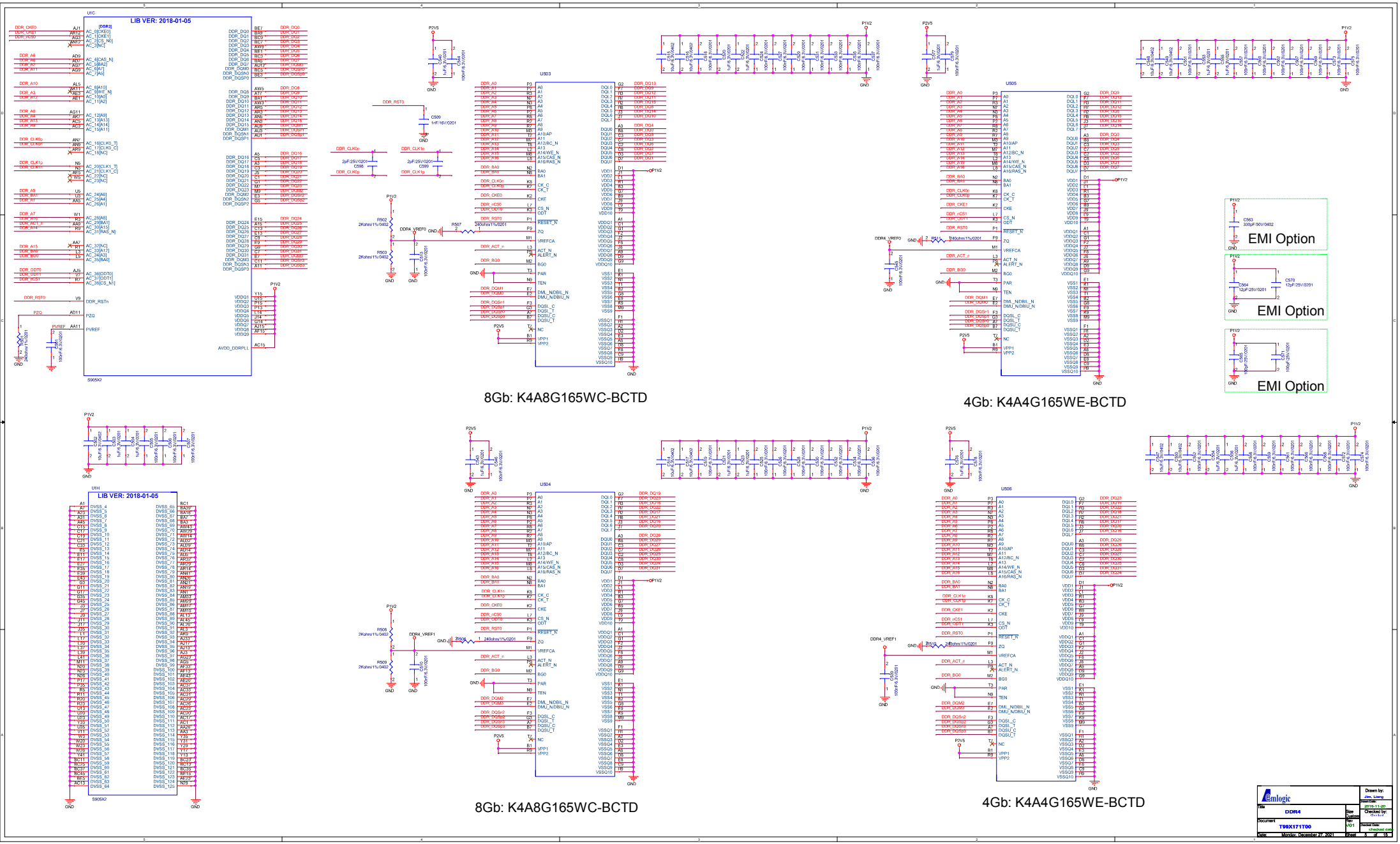

LIB VER: 2018-01-05
8Gb: K4A8G165WC-BCTD
4Gb: K4A4G165WE-BCTD
EMI Option
EMI Option
EMI Option
LIB VER: 2018-01-05
8Gb: K4A8G165WC-BCTD
4Gb: K4A4G165WE-BCTD
Amlogic
Drawn by: Jim, Liang
Date: 2018-11-20
Title: DDR4
Size: Custom
Checked by: Gerhard
Document: T99X171T00
Rev: V01
Checked Date: checked date
Date: Monday, December 27, 2021
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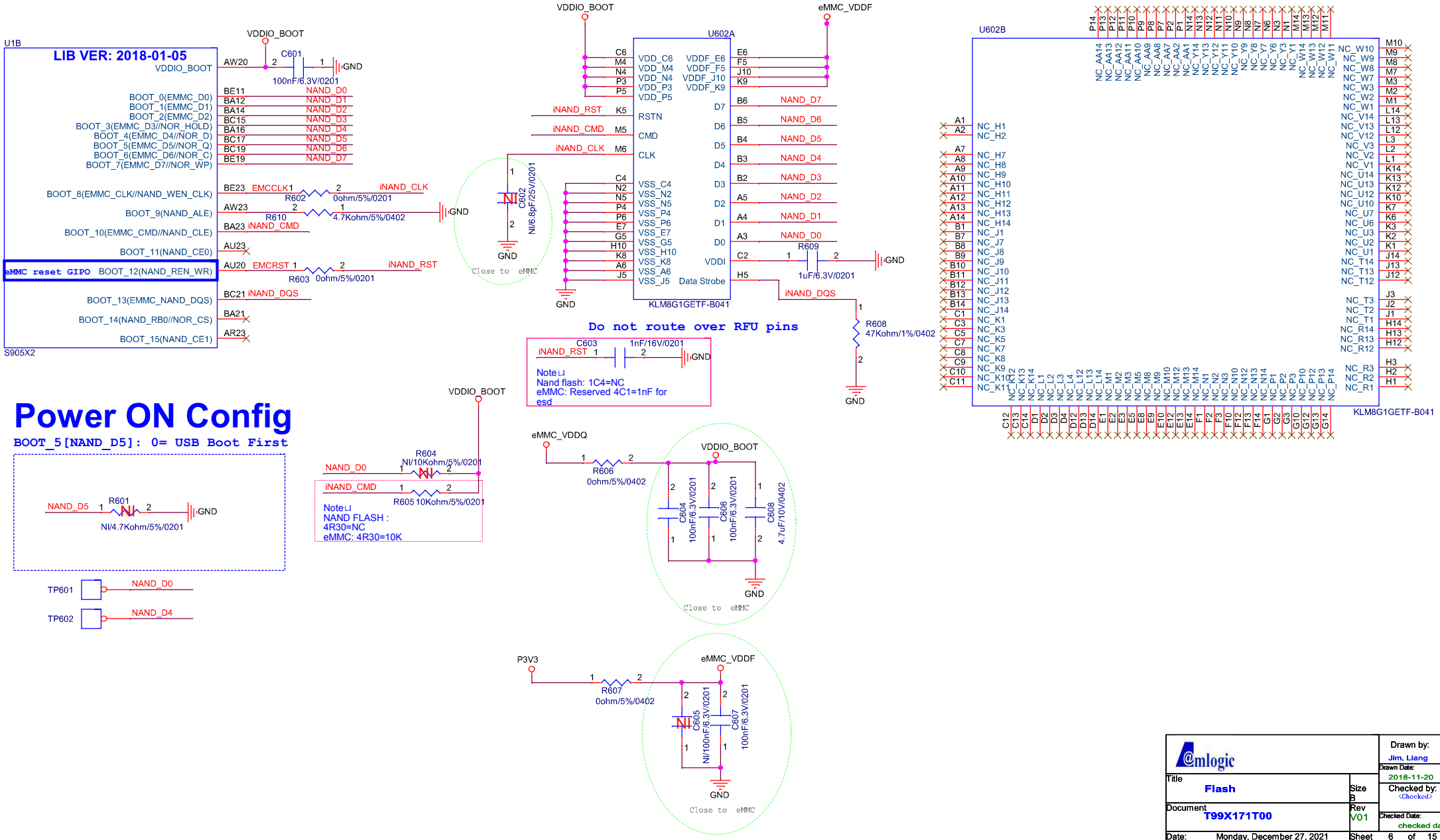
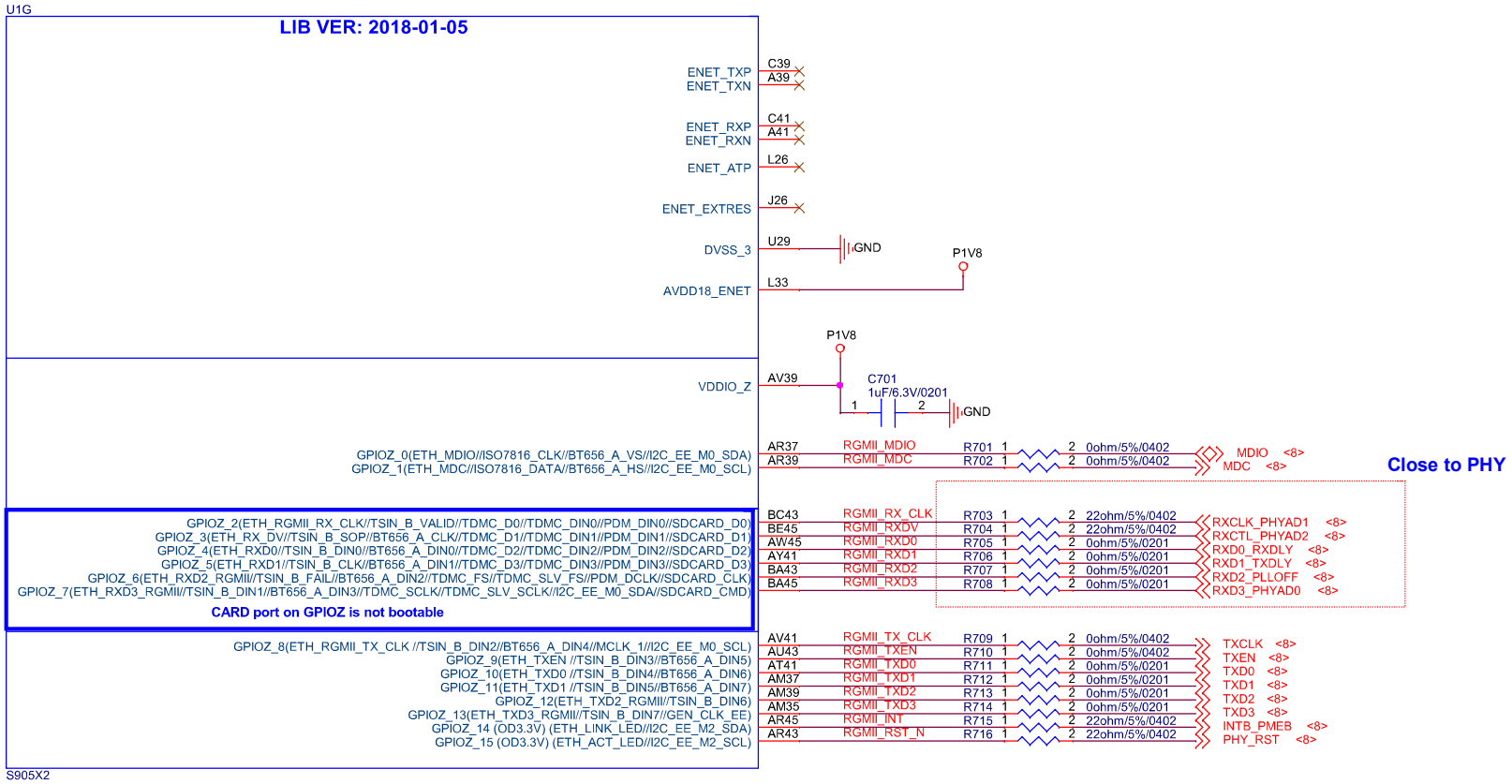
eMMC/iNAND



amlogic		Drawn by: Jim, Liang
Title: Flash	Size: B	Drawn Date: 2018-11-20
Document: T99X171T00	Rev: V01	Checked by: <Checked>
Date: Monday, December 27, 2021	Sheet 6 of 15	Checked Date: checked date



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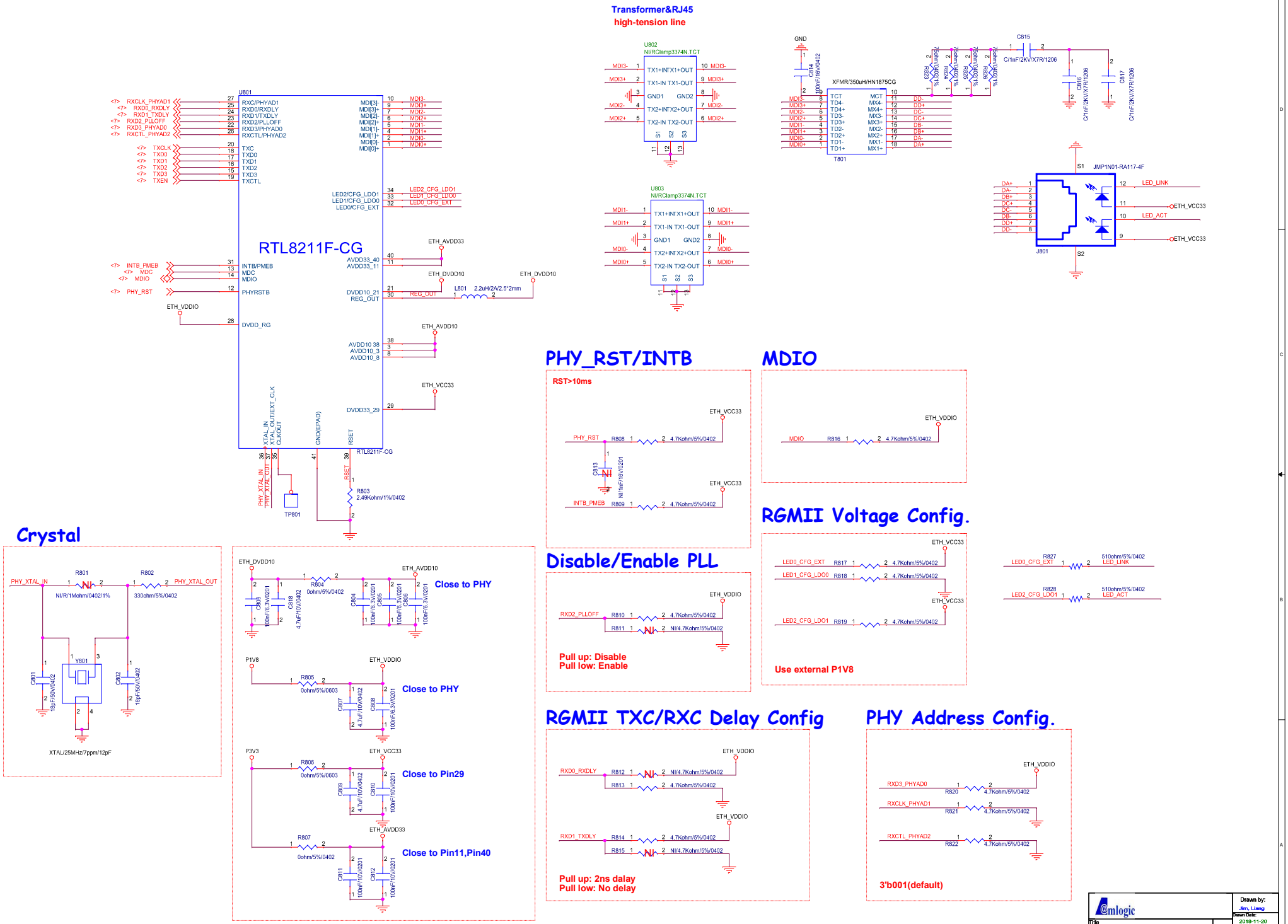
Title: Ethernet	Size: B	Drawn Date: 2018-11-20
		Checked by: <Checked>
Document: T99X171T00	Rev: V01	Checked Date: checked date
Date: Monday, December 27, 2021	Sheet 7 of 15	


Transformer&RJ45
high-tension line
U801
RTL8211F-CG
RXC/PHYAD1
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
RXCTL/PHYAD2
TXC
TXD0
TXD1
TXD2
TXD3
TXCTL
INTB/PMEB
MDC
MDIO
PHYRSTB
DVDD_RG
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
AVDD33_40
AVDD33_11
DVDD10_21
REG_OUT
AVDD10_38
AVDD10_3
AVDD10_8
DVDD33_29
XTAL_IN
XTAL_OUT/EXT_CLK
CLKOUT
GND(EPAD)
RSET
U802
NI/RClamp3374N.TCT
U803
NI/RClamp3374N.TCT
GND
XFMR/350uH/HN1875CG
T801
C815
C/1nF/2KV/X7R/1206
C816
C/1nF/2KV/X7R/1206
C817
C/1nF/2KV/X7R/1206
S1
JMP1N01-RA117-4F
J801
S2
LED_LINK
ETH_VCC33
LED_ACT
ETH_VCC33
ETH_AVDD33
ETH_DVDD10
ETH_DVDD10
L801 2.2uH/2A/2.5*2mm
ETH_VDDIO
ETH_AVDD10
ETH_VCC33
R803
2.49Kohm/1%/0402
TP801
PHY_XTAL_IN
PHY_XTAL_OUT
PHY_RST
INTB_PMEB
MDIO
RXCLK_PHYAD1
RXD0_RXDLY
RXD1_TXDLY
RXD2_PLLOFF
RXD3_PHYAD0
RXCTL_PHYAD2
TXCLK
TXD0
TXD1
TXD2
TXD3
TXEN
PHY_RST
PHY_XTAL_IN
PHY_XTAL_OUT
R801
NI/R/1Mohm/0402/1%
R802
330ohm/5%/0402
Y801
C801
18pF/50V/0402
C802
18pF/50V/0402
XTAL/25MHz/7ppm/12pF
Crystal
ETH_DVDD10
ETH_AVDD10
R804
0ohm/5%/0402
C805
100nF/6.3V/0201
C818
4.7uF/10V/0402
C804
100nF/6.3V/0201
C806
100nF/6.3V/0201
C803
100nF/6.3V/0201
Close to PHY
P1V8
ETH_VDDIO
R805
0ohm/5%/0603
C807
4.7uF/10V/0402
C808
100nF/6.3V/0201
Close to PHY
P3V3
ETH_VCC33
R806
0ohm/5%/0603
C809
4.7uF/10V/0402
C810
100nF/10V/0201
Close to Pin29
ETH_AVDD33
R807
0ohm/5%/0402
C811
100nF/10V/0201
C812
100nF/10V/0201
Close to Pin11,Pin40
PHY_RST/INTB
RST>10ms
ETH_VCC33
PHY_RST
R808
4.7Kohm/5%/0402
C813
NI/1nF/16V/0201
INTB_PMEB
R809
4.7Kohm/5%/0402
MDIO
ETH_VDDIO
MDIO
R816
4.7Kohm/5%/0402
Disable/Enable PLL
ETH_VDDIO
RXD2_PLLOFF
R810
4.7Kohm/5%/0402
R811
NI/4.7Kohm/5%/0402
Pull up: Disable
Pull low: Enable
RGMII Voltage Config.
ETH_VCC33
LED0_CFG_EXT
R817
4.7Kohm/5%/0402
LED1_CFG_LDO0
R818
4.7Kohm/5%/0402
ETH_VCC33
LED2_CFG_LDO1
R819
4.7Kohm/5%/0402
Use external P1V8
LED0_CFG_EXT
R827
510ohm/5%/0402
LED_LINK
LED2_CFG_LDO1
R828
510ohm/5%/0402
LED_ACT
RGMII TXC/RXC Delay Config
ETH_VDDIO
RXD0_RXDLY
R812
NI/4.7Kohm/5%/0402
R813
4.7Kohm/5%/0402
ETH_VDDIO
RXD1_TXDLY
R814
4.7Kohm/5%/0402
R815
NI/4.7Kohm/5%/0402
Pull up: 2ns dalay
Pull low: No delay
PHY Address Config.
ETH_VDDIO
RXD3_PHYAD0
R820
4.7Kohm/5%/0402
RXCLK_PHYAD1
R821
4.7Kohm/5%/0402
RXCTL_PHYAD2
R822
4.7Kohm/5%/0402
3'b001(default)
Amlogic
Drawn by:
Jim, Liang
Drawn Date:
2018-11-20
Checked by:
Checked
Checked Date:
checked date
Title
PHY
Size
C
Rev
V01
Document
T99X171T00
Date:
Monday, December 27, 2021
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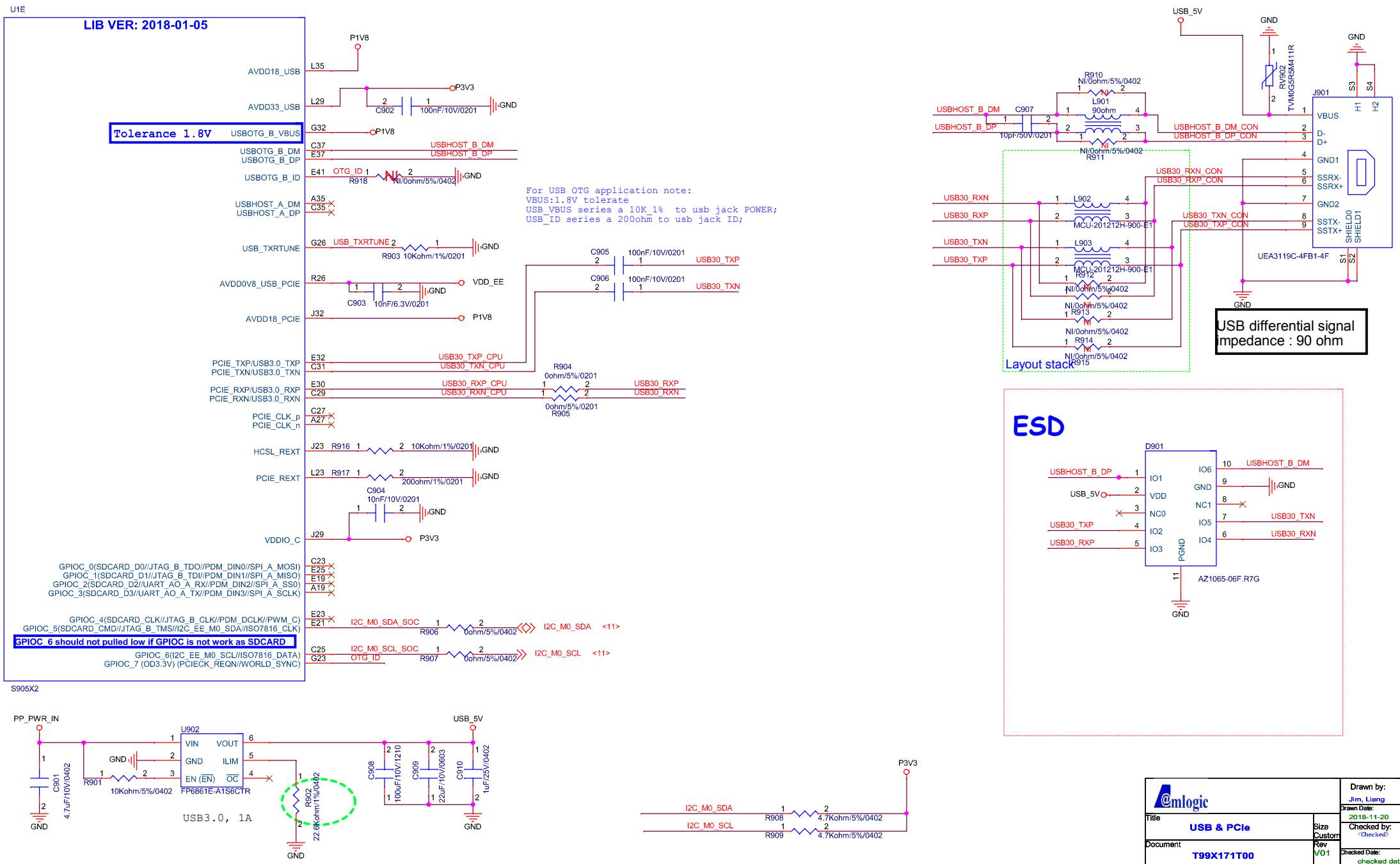
U1E
LIB VER: 2018-01-05
Tolerance 1.8V
AVDD18_USB
AVDD33_USB
USBOTG_B_VBUS
USBOTG_B_DM
USBOTG_B_DP
USBOTG_B_ID
USBHOST_A_DM
USBHOST_A_DP
USB_TXRTUNE
AVDD0V8_USB_PCIE
AVDD18_PCIE
PCIE_TXP/USB3.0_TXP
PCIE_TXN/USB3.0_TXN
PCIE_RXP/USB3.0_RXP
PCIE_RXN/USB3.0_RXN
PCIE_CLK_p
PCIE_CLK_n
HCSL_REXT
PCIE_REXT
VDDIO_C
GPIOC_0(SDCARD_D0//JTAG_B_TDO//PDM_DIN0//SPI_A_MOSI)
GPIOC_1(SDCARD_D1//JTAG_B_TDI//PDM_DIN1//SPI_A_MISO)
GPIOC_2(SDCARD_D2//UART_AO_A_RX//PDM_DIN2//SPI_A_SS0)
GPIOC_3(SDCARD_D3//UART_AO_A_TX//PDM_DIN3//SPI_A_SCLK)
GPIOC_4(SDCARD_CLK//JTAG_B_CLK//PDM_DCLK//PWM_C)
GPIOC_5(SDCARD_CMD//JTAG_B_TMS//I2C_EE_M0_SDA//ISO7816_CLK)
GPIOC_6 should not pulled low if GPIOC is not work as SDCARD
GPIOC_6(I2C_EE_M0_SCL//ISO7816_DATA)
GPIOC_7 (OD3.3V) (PCIECK_REQN//WORLD_SYNC)
S905X2
P1V8
P3V3
VDD_EE
USB30_TXP_CPU
USB30_TXN_CPU
USB30_RXP_CPU
USB30_RXN_CPU
USB30_TXP
USB30_TXN
USB30_RXP
USB30_RXN
I2C_M0_SDA_SOC
I2C_M0_SCL_SOC
OTG_ID
I2C_M0_SDA <11>
I2C_M0_SCL <11>
For USB OTG application note:
VBUS:1.8V tolerate
USB_VBUS series a 10K_1% to usb jack POWER;
USB_ID series a 200ohm to usb jack ID;
USB_5V
GND
J901
VBUS
D-
D+
GND1
SSRX-
SSRX+
GND2
SSTX-
SSTX+
SHIELD0
SHIELD1
UEA3119C-4FB1-4F
USBHOST_B_DM_CON
USBHOST_B_DP_CON
USB30_RXN_CON
USB30_RXP_CON
USB30_TXN_CON
USB30_TXP_CON
L901 90ohm
L902 MCU-201212H-900-E1
L903 MCU-201212H-900-E1
RV902 TVM0G5R5M411R
Layout stack
USB differential signal impedance : 90 ohm
ESD
D901
AZ1065-06F.R7G
PP_PWR_IN
U902
VIN
VOUT
GND
ILIM
EN (EN)
OC
FP6861E-A1S6CTR
10Kohm/5%/0402
USB3.0, 1A
22.6Kohm/1%/0402
100uF/10V/1210
22uF/10V/0603
1uF/25V/0402
4.7uF/10V/0402
I2C_M0_SDA
I2C_M0_SCL
4.7Kohm/5%/0402
Amlogic
Drawn by: Jim, Liang
Drawn Date: 2018-11-20
Checked by: 〈Checked〉
Checked Date: checked date
Title: USB & PCIe
Size: Custom
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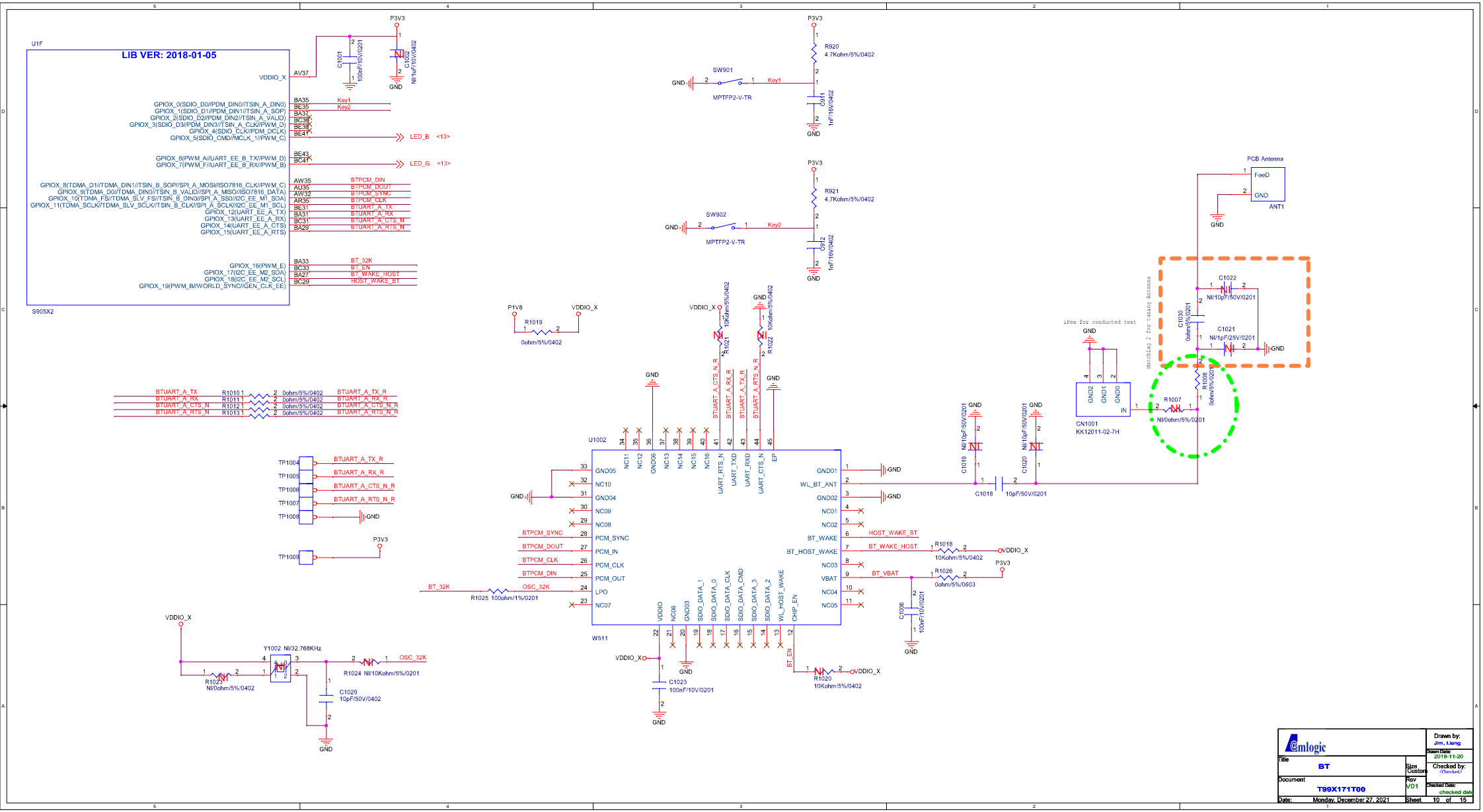
U1F
LIB VER: 2018-01-05
S905X2
VDDIO_X
AV37
BA35 Key1
BE35 Key2
BA37
BC38
BE38
BE41
LED_B <13>
BE43
BC41
LED_G <13>
AW35 BTPCM_DIN
AU35 BTPCM_DOUT
AW32 BTPCM_SYNC
AR35 BTPCM_CLK
BE31 BTUART_A_TX
BA31 BTUART_A_RX
BC31 BTUART_A_CTS_N
BA29 BTUART_A_RTS_N
BA33 BT_32K
BC33 BT_EN
BA27 BT_WAKE_HOST
BC29 HOST_WAKE_BT
GPIOX_0(SDIO_D0//PDM_DIN0//TSIN_A_DIN0)
GPIOX_1(SDIO_D1//PDM_DIN1//TSIN_A_SOP)
GPIOX_2(SDIO_D2//PDM_DIN2//TSIN_A_VALID)
GPIOX_3(SDIO_D3//PDM_DIN3//TSIN_A_CLK//PWM_D)
GPIOX_4(SDIO_CLK//PDM_DCLK)
GPIOX_5(SDIO_CMD//MCLK_1//PWM_C)
GPIOX_6(PWM_A//UART_EE_B_TX//PWM_D)
GPIOX_7(PWM_F//UART_EE_B_RX//PWM_B)
GPIOX_8(TDMA_D1//TDMA_DIN1//TSIN_B_SOP//SPI_A_MOSI//ISO7816_CLK//PWM_C)
GPIOX_9(TDMA_D0//TDMA_DIN0//TSIN_B_VALID//SPI_A_MISO//ISO7816_DATA)
GPIOX_10(TDMA_FS//TDMA_SLV_FS//TSIN_B_DIN0//SPI_A_SS0//I2C_EE_M1_SDA)
GPIOX_11(TDMA_SCLK//TDMA_SLV_SCLK//TSIN_B_CLK//SPI_A_SCLK//I2C_EE_M1_SCL)
GPIOX_12(UART_EE_A_TX)
GPIOX_13(UART_EE_A_RX)
GPIOX_14(UART_EE_A_CTS)
GPIOX_15(UART_EE_A_RTS)
GPIOX_16(PWM_E)
GPIOX_17(I2C_EE_M2_SDA)
GPIOX_18(I2C_EE_M2_SCL)
GPIOX_19(PWM_B//WORLD_SYNC//GEN_CLK_EE)
P3V3
C1001 100nF/10V/0201
C1002 NI/1uF/10V/0402
GND
SW901
MPTFP2-V-TR
R920 4.7Kohm/5%/0402
C3011 1nF/16V/0402
SW902
MPTFP2-V-TR
R921 4.7Kohm/5%/0402
C3012 1nF/16V/0402
PCB Antenna
FeeD
GND
ANT1
C1022 NI/10pF/50V/0201
C1021 NI/1pF/25V/0201
C1030 0ohm/5%/0201
R1008 0ohm/5%/0201
Matching 2 for tuning Antenna
iPex for conducted test
GND2 GND1 GND0 IN
CN1001
KK12011-02-7H
R1007 NI/0ohm/5%/0201
P1V8
R1019 0ohm/5%/0402
VDDIO_X
R1021 10Kohm/5%/0402
R1022 10Kohm/5%/0402
BTUART_A_TX R1010 0ohm/5%/0402 BTUART_A_TX_R
BTUART_A_RX R1011 0ohm/5%/0402 BTUART_A_RX_R
BTUART_A_CTS_N R1012 0ohm/5%/0402 BTUART_A_CTS_N_R
BTUART_A_RTS_N R1013 0ohm/5%/0402 BTUART_A_RTS_N_R
TP1004 BTUART_A_TX_R
TP1005 BTUART_A_RX_R
TP1006 BTUART_A_CTS_N_R
TP1007 BTUART_A_RTS_N_R
TP1008
TP1009
U1002
W511
GND01 WL_BT_ANT GND02 NC01 NC02 BT_WAKE BT_HOST_WAKE NC03 VBAT NC04 NC05
GND05 NC10 GND04 NC09 NC08 PCM_SYNC PCM_IN PCM_CLK PCM_OUT LPO NC07
NC11 NC12 GND06 NC13 NC14 NC15 NC16 UART_RTS_N UART_TXD UART_RXD UART_CTS_N EP
VDDIO GND03 SDIO_DATA_1 SDIO_DATA_0 SDIO_DATA_CLK SDIO_DATA_CMD SDIO_DATA_3 SDIO_DATA_2 WL_HOST_WAKE CHIP_EN
BTPCM_SYNC BTPCM_DOUT BTPCM_CLK BTPCM_DIN OSC_32K
BT_32K R1025 100ohm/1%/0201
HOST_WAKE_BT
BT_WAKE_HOST R1018 10Kohm/5%/0402
BT_VBAT R1026 0ohm/5%/0603
C1019 NI/10pF/50V/0201
C1018 10pF/50V/0201
C1020 NI/10pF/50V/0201
C1006 100nF/10V/0201
C1023 100nF/10V/0201
BT_EN R1020 10Kohm/5%/0402
Y1002 NI/32.768KHz
R1023 NI/0ohm/5%/0402
R1024 NI/10Kohm/5%/0201
C1029 10pF/50V/0402
Amlogic
Title BT
Document T99X171T00
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Drawn Date: 2018-11-20
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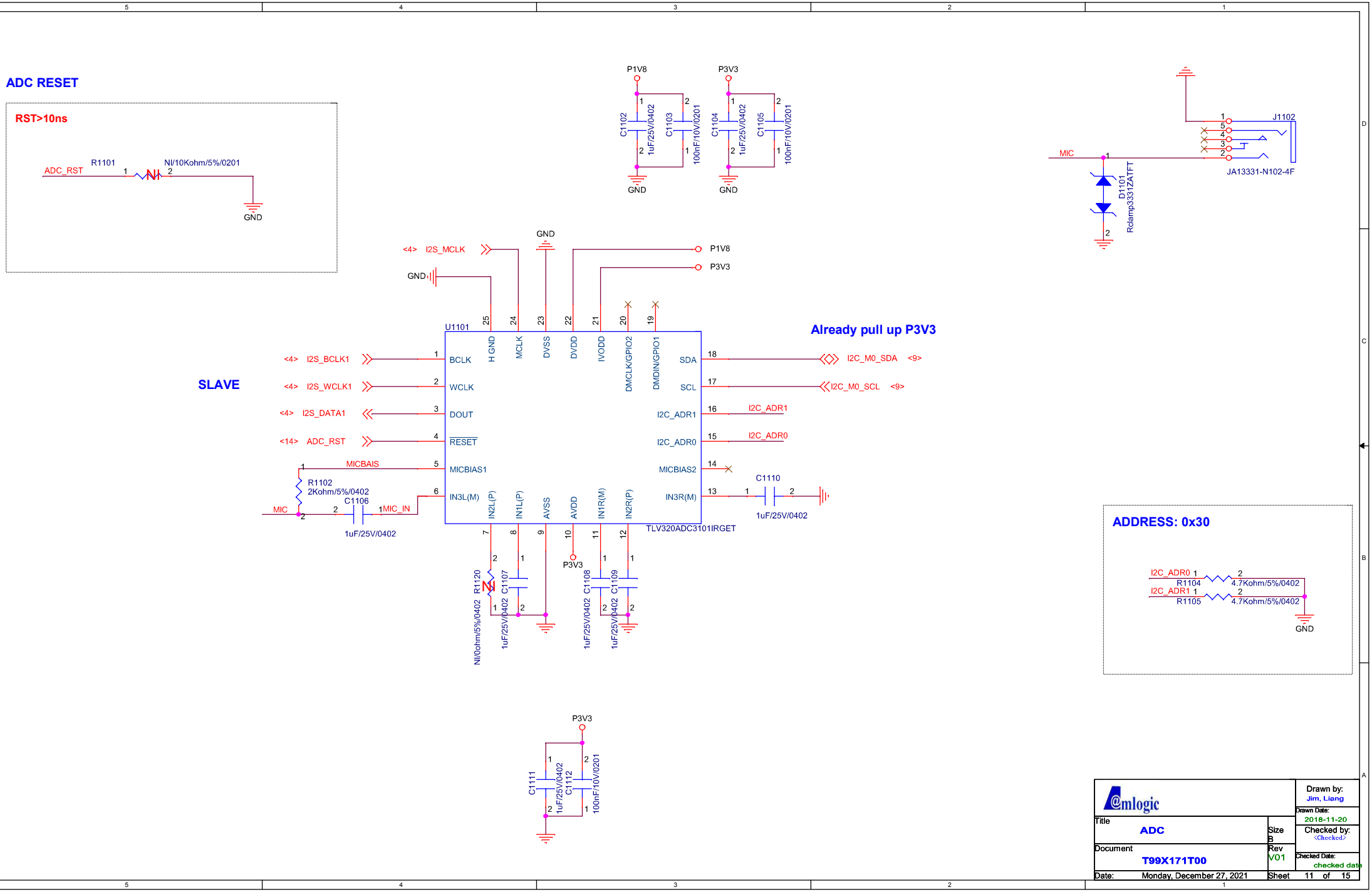
ADC RESET
RST>10ns
ADC_RST
R1101
NI/10Kohm/5%/0201
GND
P1V8
P3V3
C1102
1uF/25V/0402
C1103
100nF/10V/0201
C1104
1uF/25V/0402
C1105
100nF/10V/0201
GND
GND
J1102
MIC
D1101
Rclamp3331ZATFT
JA13331-N102-4F
<4> I2S_MCLK
GND
GND
P1V8
P3V3
U1101
SLAVE
Already pull up P3V3
<4> I2S_BCLK1
<4> I2S_WCLK1
<4> I2S_DATA1
<14> ADC_RST
MICBAIS
R1102
2Kohm/5%/0402
MIC
C1106
1uF/25V/0402
MIC_IN
BCLK
WCLK
DOUT
RESET
MICBIAS1
IN3L(M)
H GND
MCLK
DVSS
DVDD
IVODD
DMCLK/GPIO2
DMDIN/GPIO1
SDA
SCL
I2C_ADR1
I2C_ADR0
MICBIAS2
IN3R(M)
I2C_M0_SDA <9>
I2C_M0_SCL <9>
I2C_ADR1
I2C_ADR0
C1110
1uF/25V/0402
IN2L(P)
IN1L(P)
AVSS
AVDD
IN1R(M)
IN2R(P)
TLV320ADC3101IRGET
R1120
NI/0ohm/5%/0402
C1107
1uF/25V/0402
P3V3
C1108
1uF/25V/0402
C1109
1uF/25V/0402
ADDRESS: 0x30
I2C_ADR0
R1104
4.7Kohm/5%/0402
I2C_ADR1
R1105
4.7Kohm/5%/0402
GND
P3V3
C1111
1uF/25V/0402
C1112
100nF/10V/0201
Amlogic
Drawn by:
Jim, Liang
Drawn Date:
2018-11-20
Checked by:
<Checked>
Checked Date:
checked date
Title
ADC
Size
B
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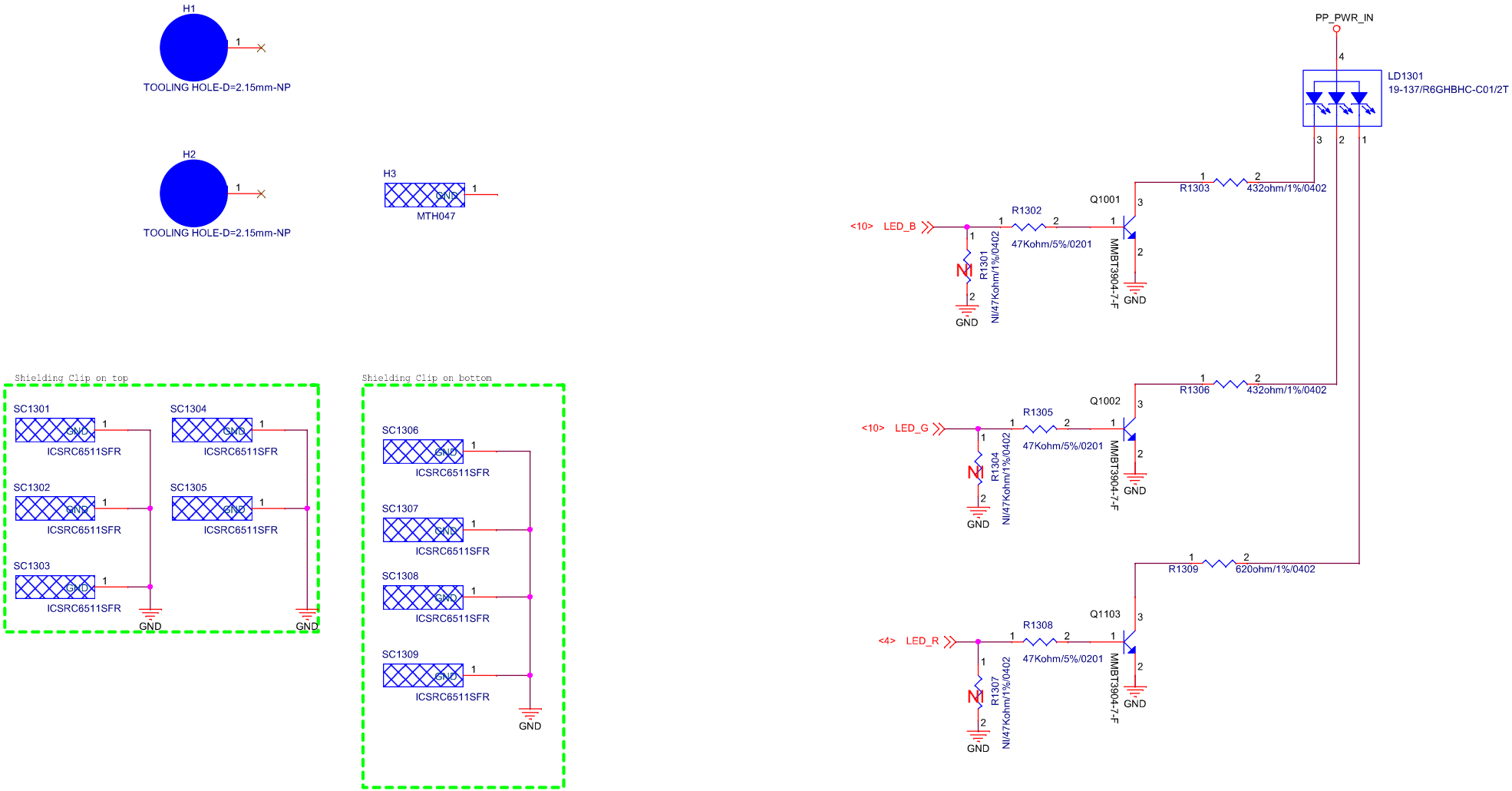
Amlogic			Drawn by: Jim, Liang
			Drawn Date: 2018-11-20
Title: DSP	Size: B		Checked by: <Checked>
Document: T99X171T00	Rev: V01		Checked Date: checked date
Date: Monday, December 27, 2021	Sheet 12 of 15		



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Title: LED/CLIP	Size: B	Drawn Date: 2018-11-20
		Checked by: <Checked>
Document: T99X171T00	Rev: V01	Checked Date: checked date
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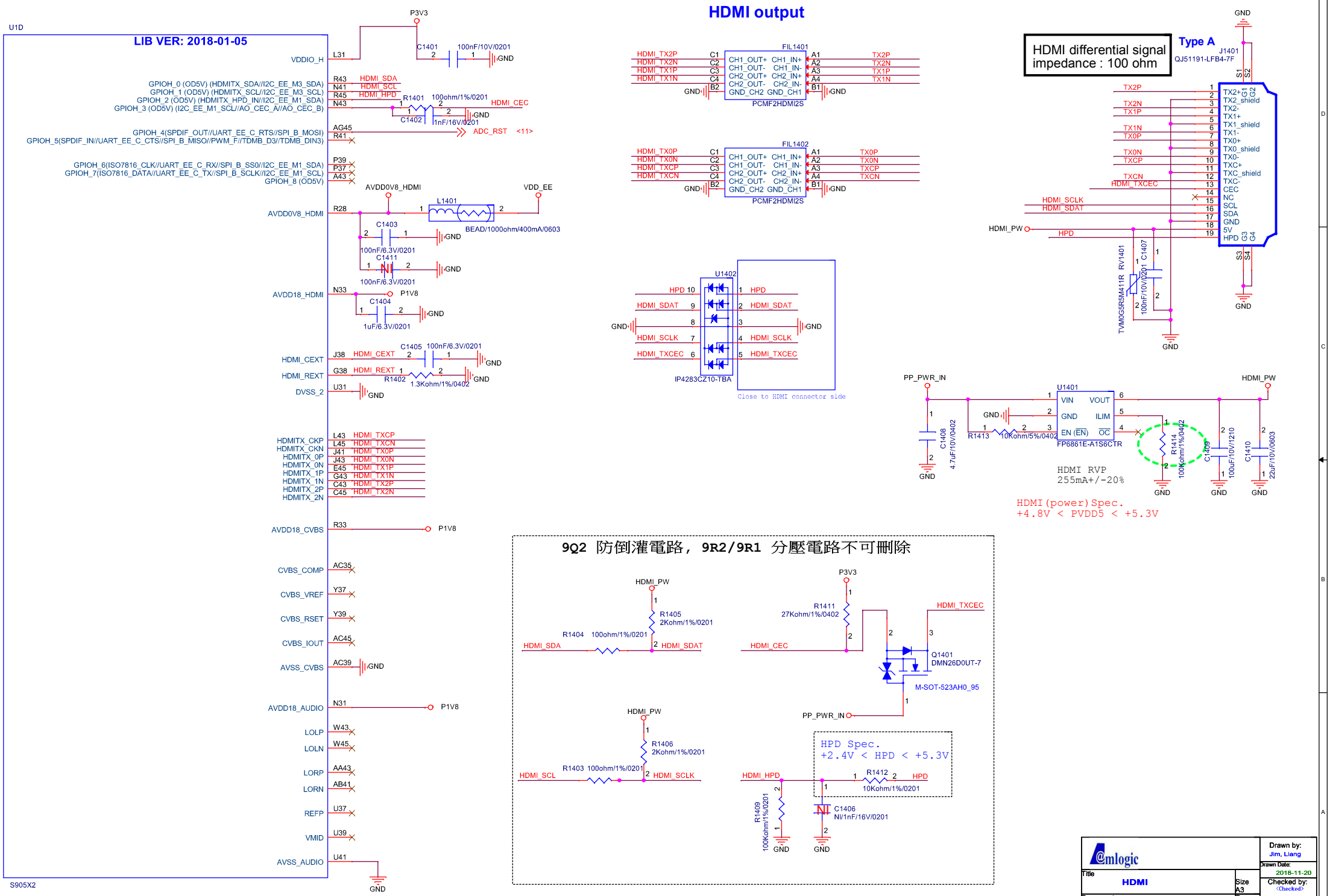
HDMI output



Amlogic	Drawn by: Jim, Liang	
Title: HDMI	Size A3	Drawn Date: 2018-11-20
Document: T99X171T00	Rev V01	Checked by: <Checked>
Date: Monday, December 27, 2021	Sheet 14 of 15	Checked Date: checked date

Version	Change List	Date
001	First version of T99X171T00	2018/11/01

Version	Change List	Date
002	First version of T99X171T00	2019/03/15

Page 3.
1. OVP and OCP: Change D301 and F301 to TPS25200 solution

2. P1V8 LDO ripple: Change U303 and 306 from 027.01421.005 to JSTLV75518PDBV

3. P2V5 LDO ripple: Change U303 and 306 from 027.01437.005 to JSTLV75525PDBV

Page 4.
4. Slove I2S overshoot and undershoot:Change R412, R413, R414, R415 from 0ohm to 49.9ohm

5. Support wake on BT: Change Net BT_WAKE_HOST fom GPIOX_18 to GPIOAO_2

Page 7.
6. No use for reserve EMI: Delete C702 22p

Page 8.
7. Xtal 25M: Change R802 from 0ohm to 330ohm

8. For phy bringup: add C818 4.7u

9. RGMII TXC/RXC Delay Config: Tx 2ns dealy, pop R814 and R815 nopop
Rx no dealy, pop R813 and R812 nopop

Page 9.

10. USB OTG_ID control pin change to open drain pin: Change OUG_ID from GPIOC_1 to GPIOC_7

Page 10.
11. Xtal 20M: Change C1015 and C1016 from 18p to 8.2p

12. LED (B) change default pull up pin: change LED_B from GPIOAO_11 to GPIO_X5

13. LED (G) change default pull up pin: change LED_G from GPIO_X6 to GPIO_X7

Page 11.
14. ADC change AGND ro GND: Delete R1103, R1106, R1107, R1108, C1113

Page 14.
15. Change HDMI I2C pull up from PP_PWR_IN to HDMI_PW

Amlogic		Drawn by: Jim, Liang
Title: Revision History	Size: A3	Drawn Date: 2018-11-20
Document: T99X171T00	Rev: V01	Checked by: <Checked>
Date: Monday, December 27, 2021	Sheet 15 of 15	Checked Date: checked date