

Signal Integrity Simulation Report

Project: T99X171T00 DDR4-2666
Post-simulation Results
Date: 2019/03/25

	Approved	Author
BY	Siangwei.sw.Wan g	Neo.ih.tseng



Simulation Conditions

- **Simulation board file:** T99X171T00_005A.brd
- **Simulation model:**

Component	IBIS / Spice Model Name	Version / Provider
Controller	S905x2_v1.ibs	Amlogic
DRAM	i_k4a4g165we_bcxx_jan29.ibs	Samsung
	i_k4a8g165wc-bcxx_jul04.ibs	Samsung

- **Pre-requisite:**

Concerned factor	Not concerned
XTALK	Trace temperature
TX drive strength & RX ODT	Manufacture variation
Power SSN to SI effects	

Note:

1. The XTALK have include nets with coupled voltage greater than 120mV, and considered in waveform simulation with sensitive aggressors.
2. The simulation are from die-to-die (include package) results.

- **Stackup:**

Layer Name	Type	Usage	Thickness mils	Er	Test Width mils	Z0 ohm
DIE_001	Dielectric	Solder Mask	0.4	4.2		
TOP	Metal	Signal	1.8	<Auto>	3.99	55
DIE_003	Dielectric	Substrate	3.2	3.91		
MID1_L2_	Metal	Plane	1.2	<Auto>	16	56.3
DIE_005	Dielectric	Substrate	4	3.95		
MID2_L3_	Metal	Signal	1.2	<Auto>	3.99	55
DIE_007	Dielectric	Substrate	15.7	3.3		
MID3_L4_	Metal	Plane	1.2	<Auto>	16	26.4
DIE_009	Dielectric	Substrate	4	3.95		
MID4_L5_	Metal	Plane	1.2	<Auto>	16	28
DIE_011	Dielectric	Substrate	3.2	3.91		
BOTTOM	Metal	Signal	1.8	<Auto>	3.99	55
DIE_013	Dielectric	Solder Mask	0.4	4.2		

JEDEC standard for DDR4(1/2)

- ADD and CMD AC/DC threshold :**

[Table 7] Single-ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666		Unit
		Min.	Max.	Min.	Max.	
$V_{IH,CA}(DC75)$	DC input logic high	$V_{REFCA} + 0.075$	VDD	-	-	V
$V_{IH,CA}(DC65)$		-	-	$V_{REFCA} + 0.065$	VDD	
$V_{IL,CA}(DC75)$	DC input logic low	VSS	$V_{REFCA} - 0.075$	-	-	V
$V_{IL,CA}(DC65)$		-	-	VSS	$V_{REFCA} - 0.065$	
$V_{IH,CA}(AC100)$	AC input logic high	$V_{REF} + 0.1$	Note 2	-	-	V
$V_{IH,CA}(AC90)$		-	-	$V_{REF} + 0.09$	Note 2	
$V_{IL,CA}(AC100)$	AC input logic low	Note 2	$V_{REF} - 0.1$	-	-	V
$V_{IL,CA}(AC90)$		-	-	Note 2	$V_{REF} - 0.09$	
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 \times VDD$	$0.51 \times VDD$	$0.49 \times VDD$	$0.51 \times VDD$	V

$$tD(\text{margin}) = [tD - \text{Initial Delay Delta}] - [tD(\text{base}) + d(tD)]$$

ADD/CMD timing margin	Setup time	Hold time
tD	From simulation	
Initial Delay Delta	6	6
tD(base), Base Setup/Hold Time	55	80
d(tD), max derate time delta	0	0

[Table 55] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2666

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing													
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	55	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	145	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	80	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	145	-	ps	

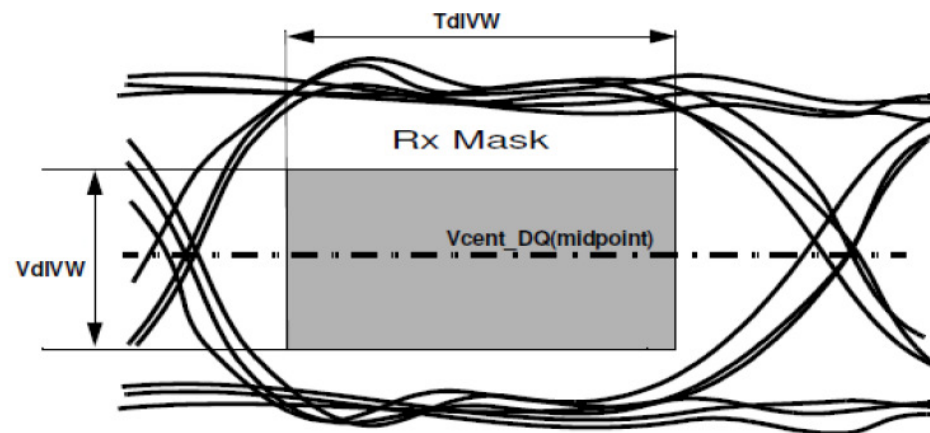
Note :

1. The ADD's threshold reference DDR specification "K4A4G165WE-BCTD" page 11, Table 7.
2. The ADD Setup/Hold time value reference DDR specification "K4A4G165WE-BCTD" page 58, Table 58.

JEDEC standard for DDR4(2/2)

- DATA timing analysis :**

The DQ input receiver compliance mask for voltage and timing is shown in the figure. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.



Symbol	Parameter	1600/1866/2133		2400		2666		Unit
		min	max	min	max	min	max	
VdIVW	Rx Mask voltage - pk-pk	-	136	-	130	-	120	mV
TdIVW	Rx timing window	-	0.2	-	0.2	-	0.22	UI*

Note :

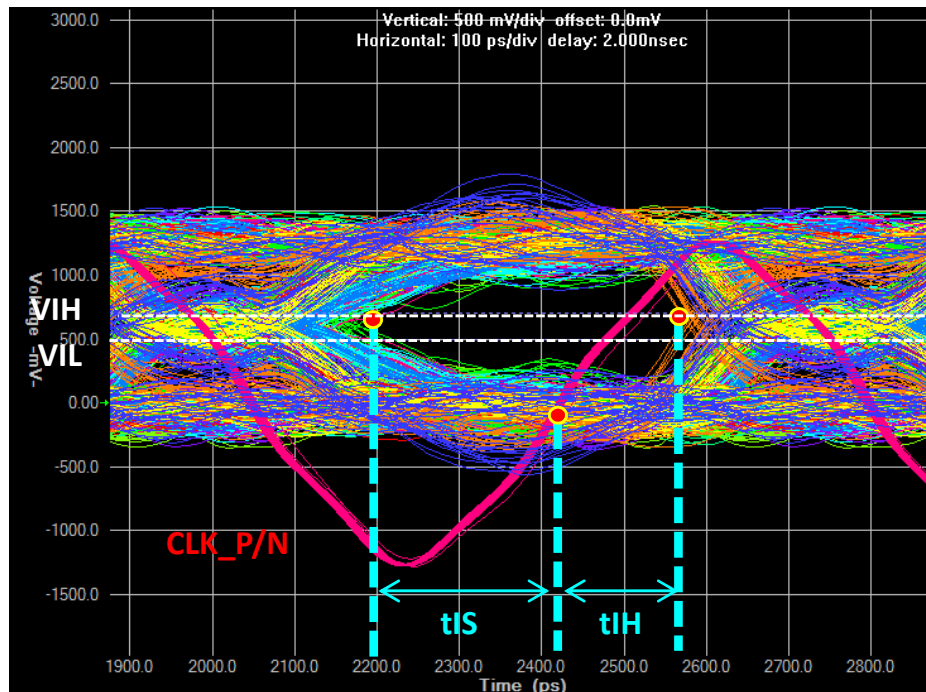
1. Rx mask reference DDR specification “K4A4G165WE-BCTD” page 67, Table 54.

Post-Layout Simulation

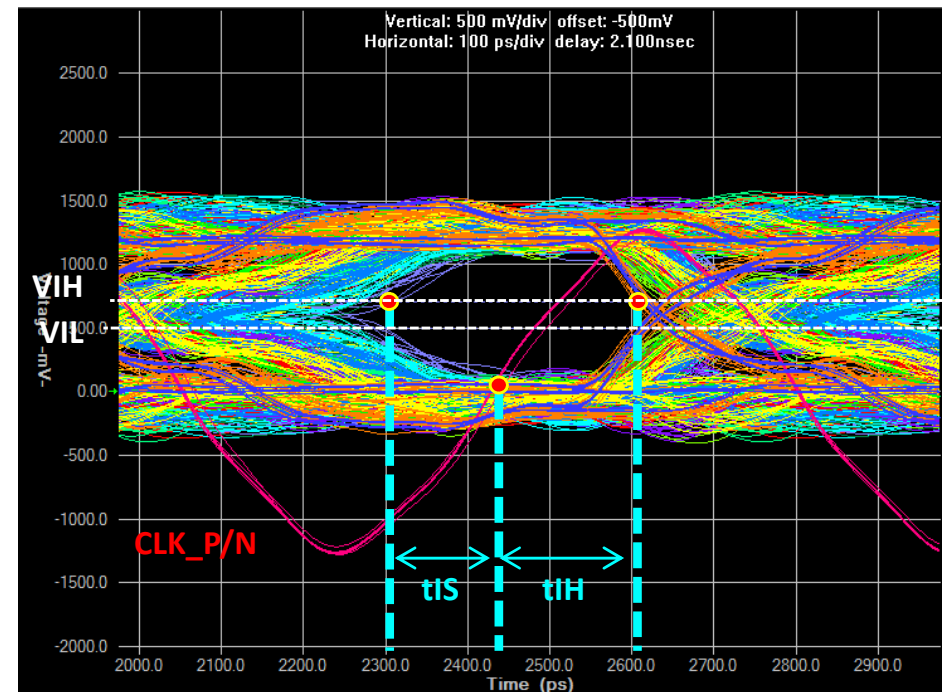
- **CK v.s CA Write**
 - Simulation Waveform & Timing Margin Analysis
- **DQS v.s DQ Write**
 - Simulation Waveform & Timing Margin Analysis
- **DQS v.s DQ Read**
 - Simulation Waveform & Timing Margin Analysis

ADD/CMD/CTRL Simulation Waveform(typ)

U1 Driver → DDR U503 Received @die:
CLK vs. ADD, CMD, CTRL



U1 Driver → DDR U505 Received @die:
CLK vs. ADD, CMD, CTRL

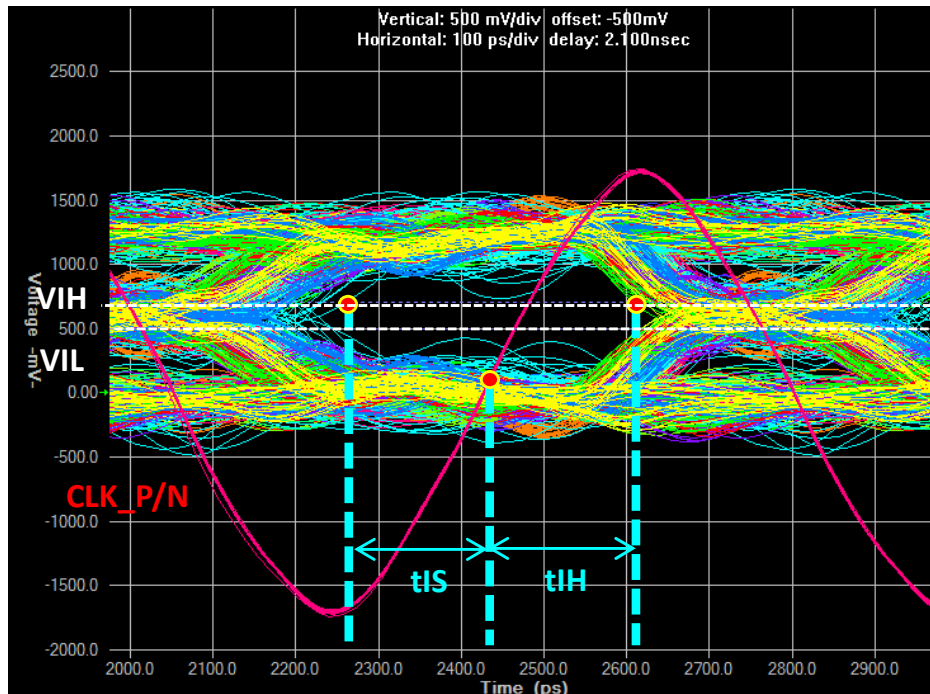


Note :

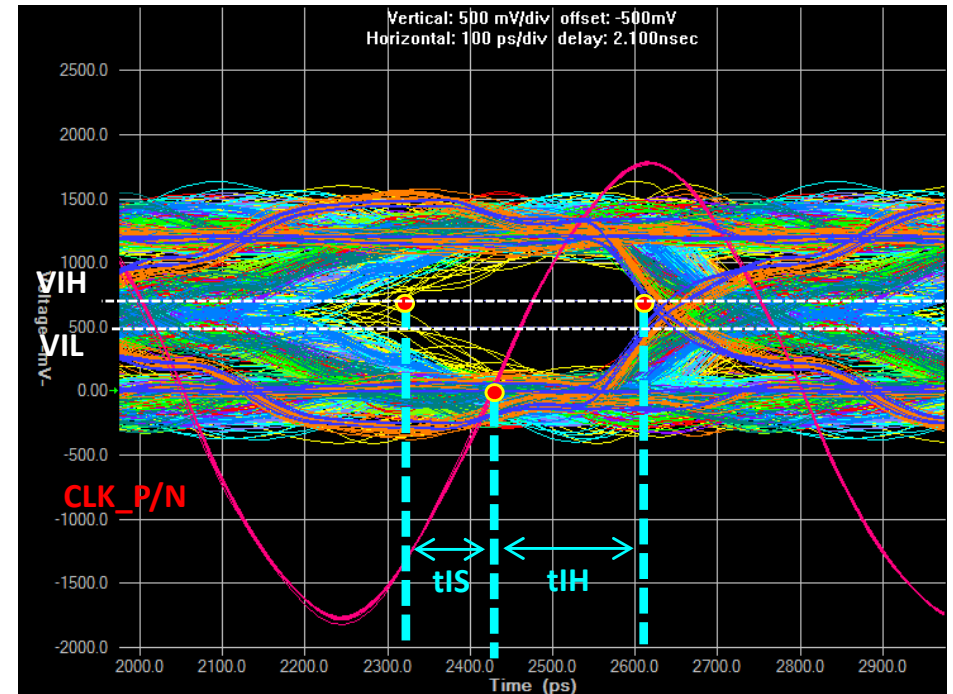
The purpose of this simulation is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification

ADD/CMD/CTRL Simulation Waveform(typ)

U1 Driver → DDR U504 Received @die:
CLK vs. ADD, CMD, CTRL



U1 Driver → DDR U506 Received @die:
CLK vs. ADD, CMD, CTRL



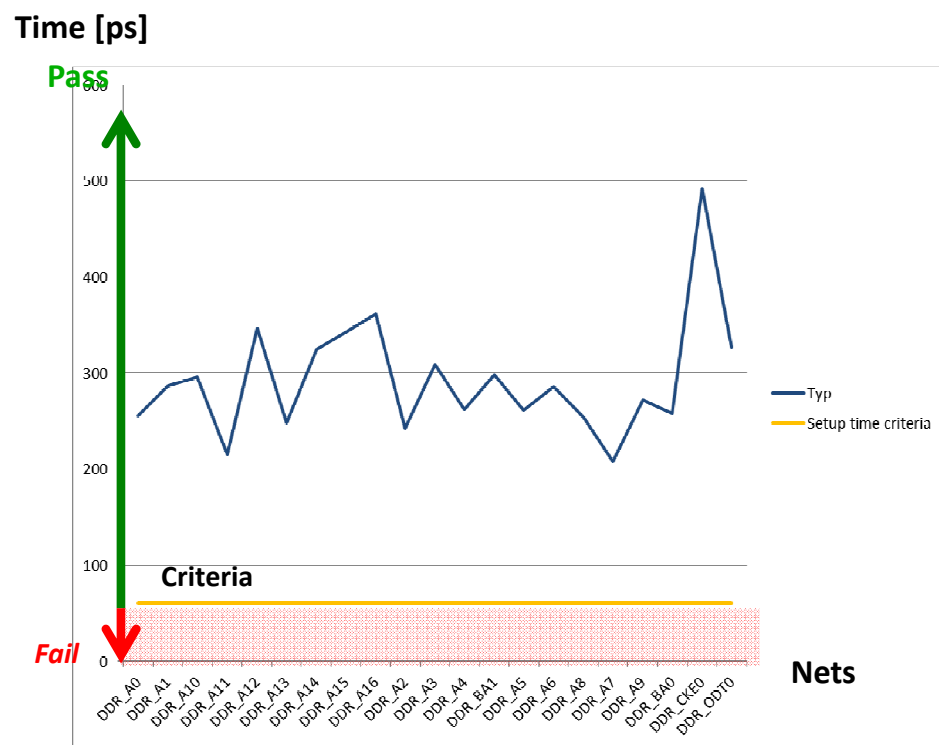
Note :

The purpose of this simulation is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification

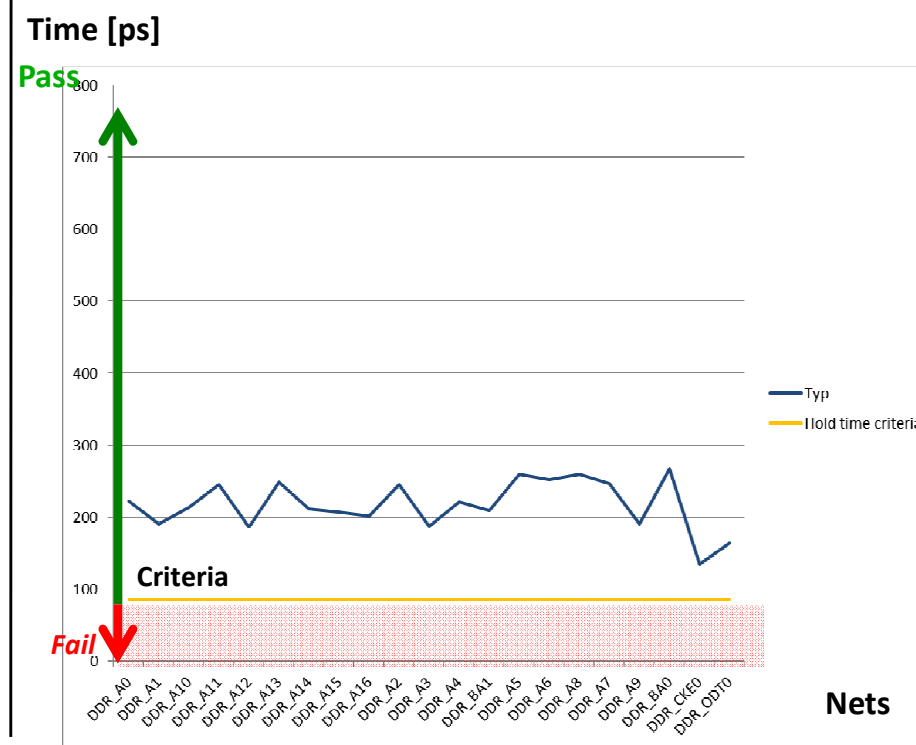
CK vs. ADD/CMD/CTRL Timing Budget @DDR U503

Pass

Setup Time Margin (tIS)



Hold Time Margin (tIH)



Note:

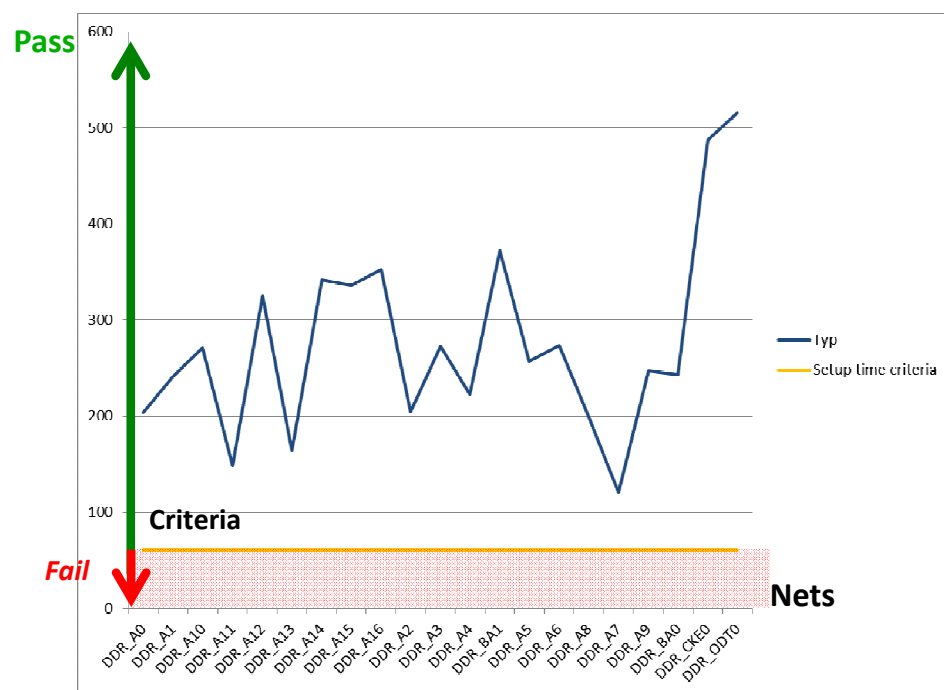
1. Based on CPU drive strength "mal4drv20_d4_30", and DDR "ADDR_PIN" on die termination.
2. Both setup/hold time margin should be positive and within specification limit to have enough margin in each nets for pass condition.

CK vs. ADD/CMD/CTRL Timing Budget @DDR U505

Pass

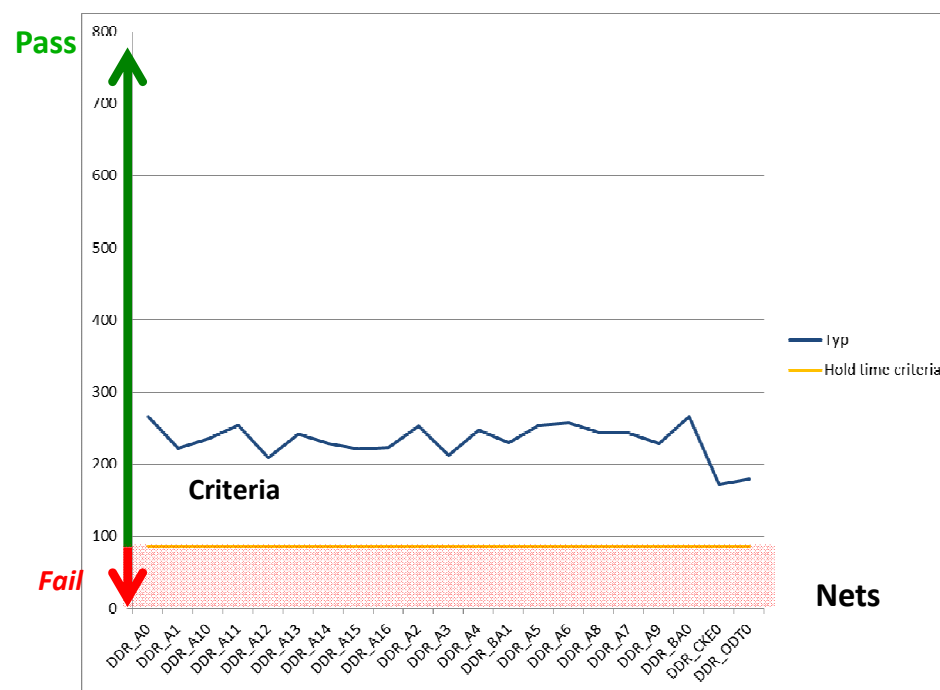
Setup Time Margin (tIS)

Time [ps]



Hold Time Margin (tIH)

Time [ps]



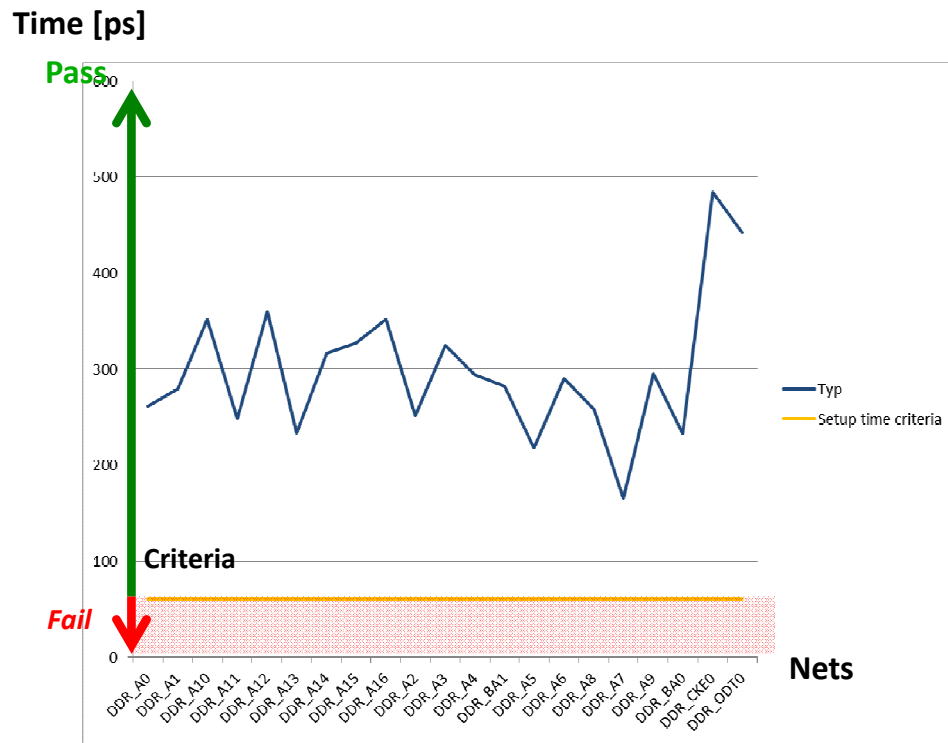
Note:

1. Based on CPU drive strength "mal4drv20_d4_30", and DDR "ADDR_PIN" on die termination.
2. Both setup/hold time margin should be positive and within specification limit to have enough margin in each nets for pass condition.

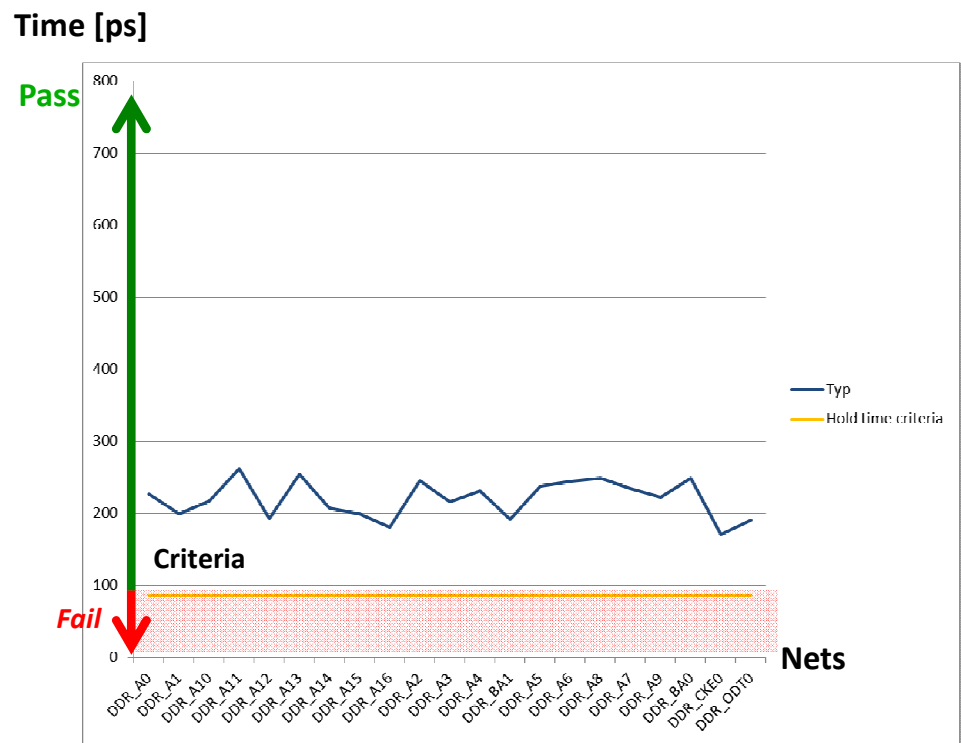
CK vs. ADD/CMD/CTRL Timing Budget @DDR U504

Pass

Setup Time Margin (tIS)



Hold Time Margin (tIH)



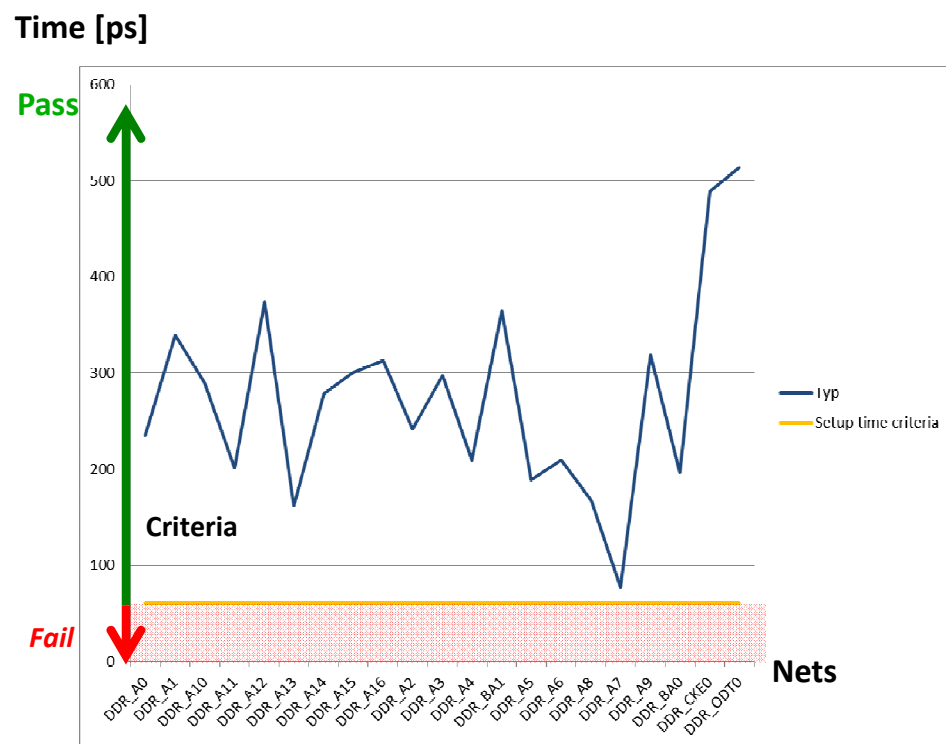
Note:

1. Based on CPU drive strength "mal4drv20_d4_30", and DDR "ADDR_PIN" on die termination.
2. Both setup/hold time margin should be positive and within specification limit to have enough margin in each nets for pass condition.

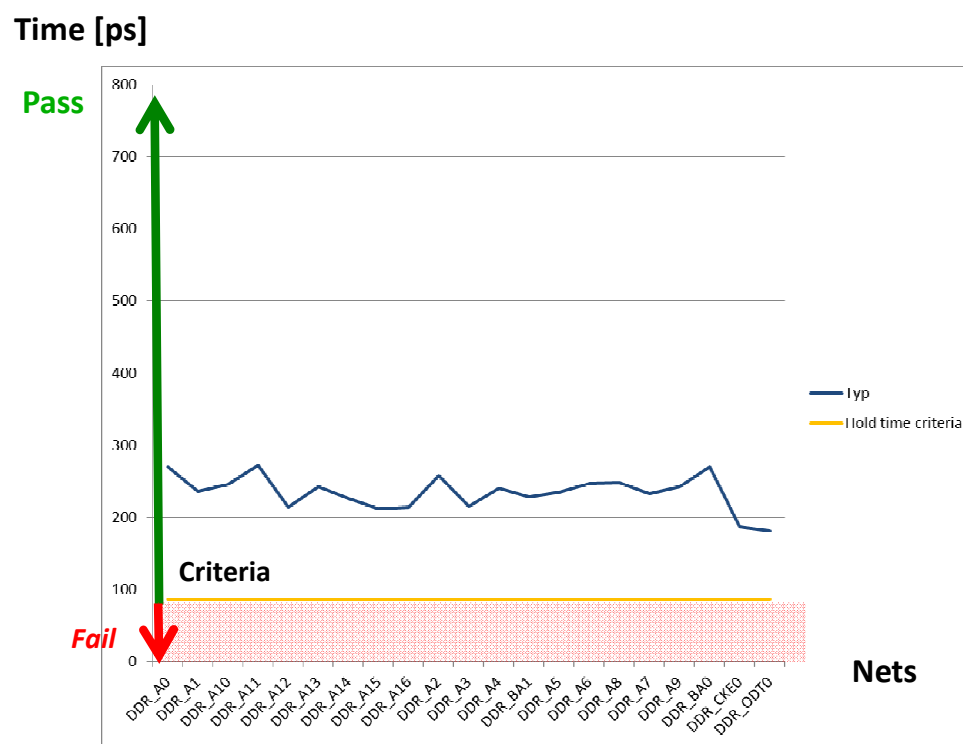
CK vs. ADD/CMD/CTRL Timing Budget @DDR U506

Pass

Setup Time Margin (tIS)



Hold Time Margin (tIH)



Note:

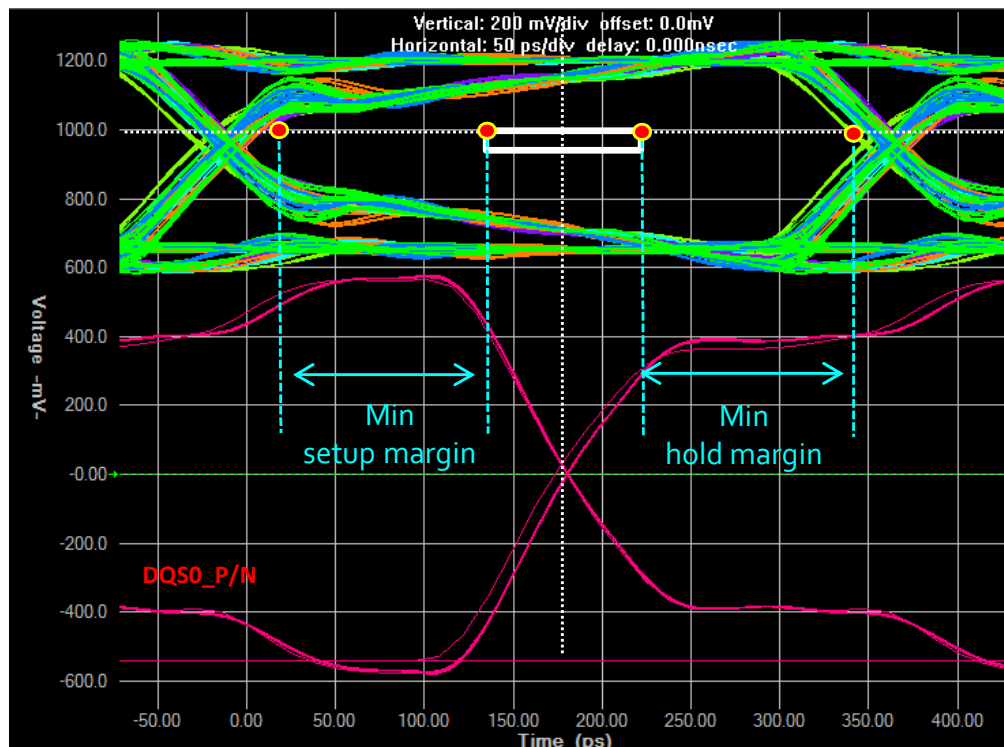
1. Based on CPU drive strength "mal4drv20_d4_30", and DDR "ADDR_PIN" on die termination.
2. Both setup/hold time margin should be positive and within specification limit to have enough margin in each nets for pass condition.

Post-Layout Simulation

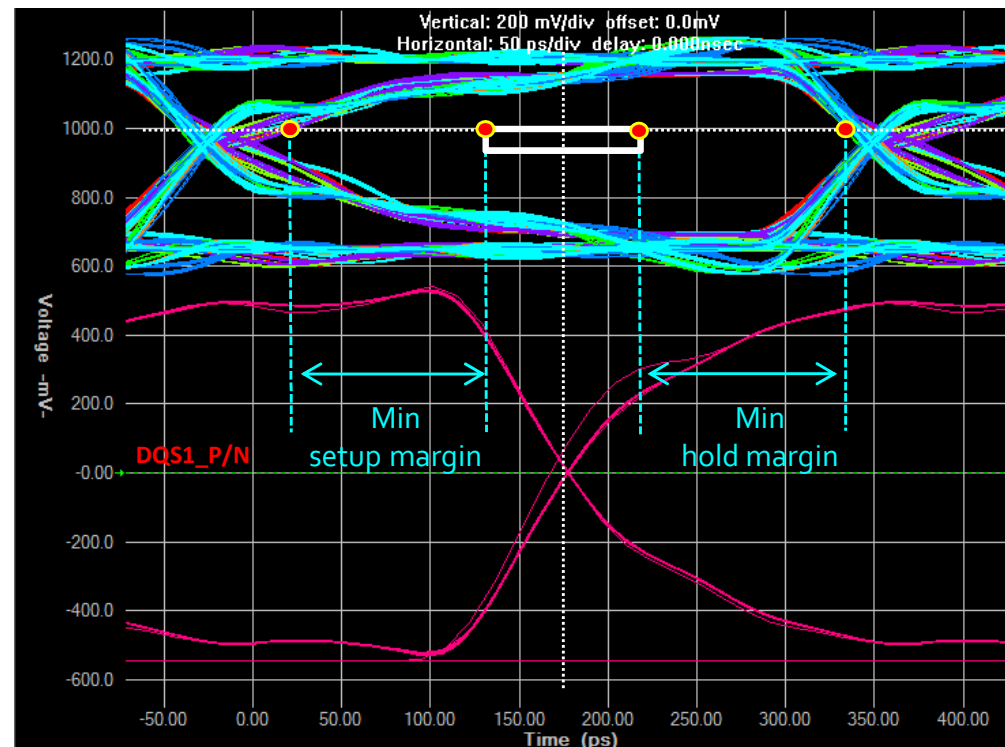
- **CK v.s CA Write**
 - Simulation Waveform & Timing Margin Analysis
- **DQS v.s DQ Write**
 - Simulation Waveform & Timing Margin Analysis
- **DQS v.s DQ Read**
 - Simulation Waveform & Timing Margin Analysis

Data Write Simulation Waveform(typ) @DDR U503

DQS0 vs. DQ[0:7], DMASK0



DQS1 vs. DQ[8:15], DMASK1

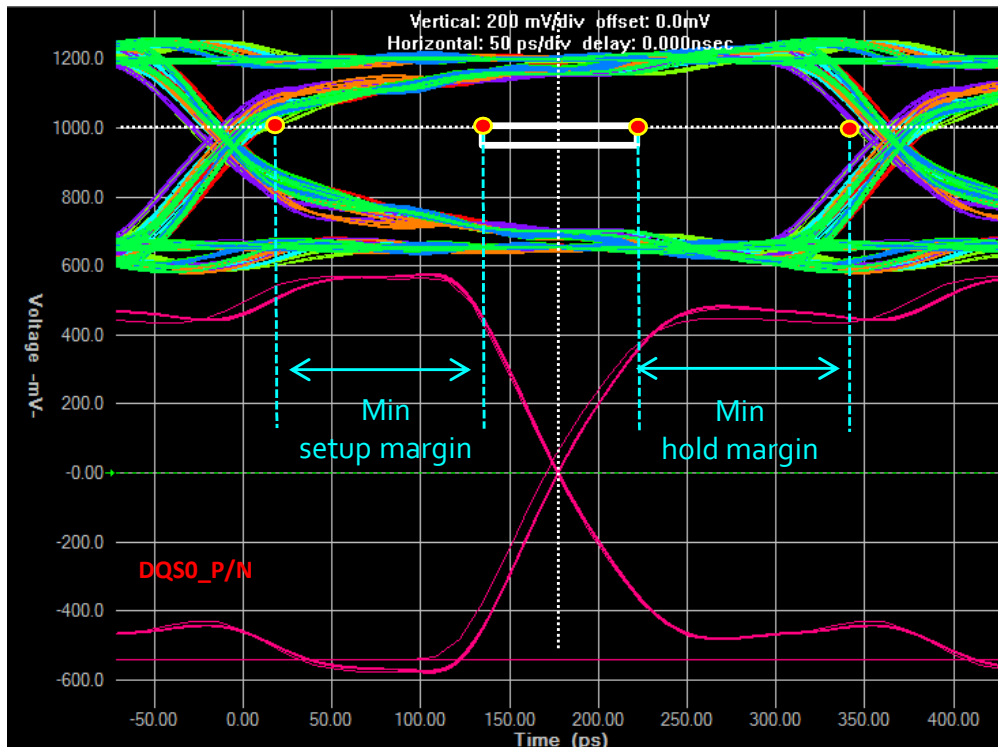


Note :

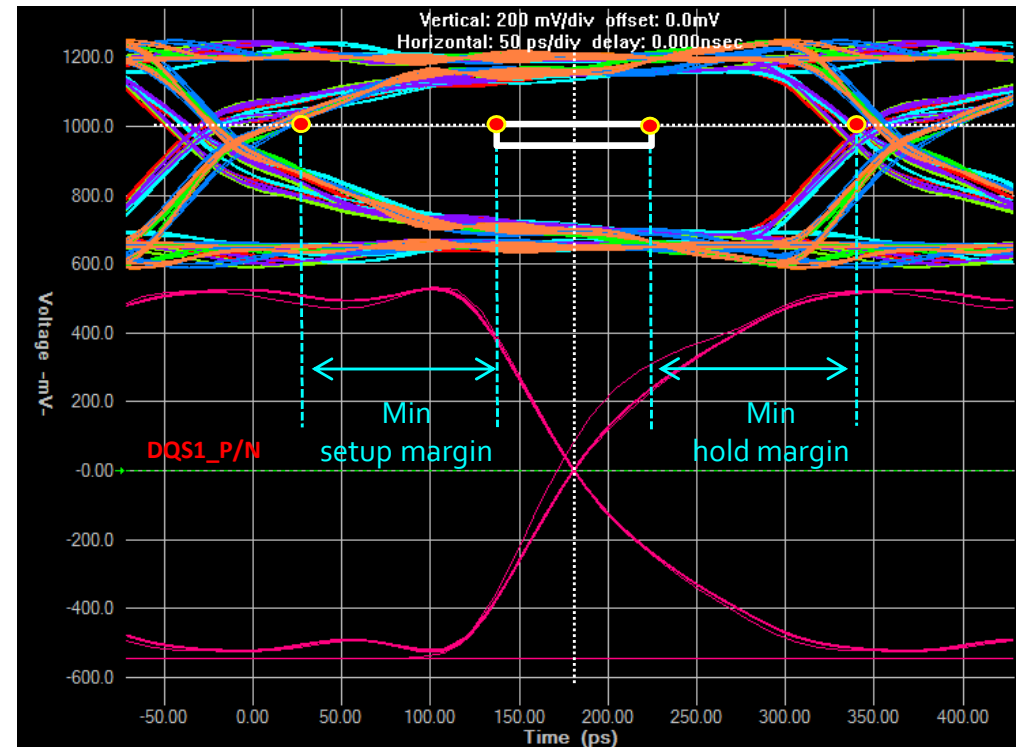
Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

Data Write Simulation Waveform(typ) @DDR U505

DQS0 vs. DQ[0:7], DMASK0



DQS1 vs. DQ[8:15], DMASK1

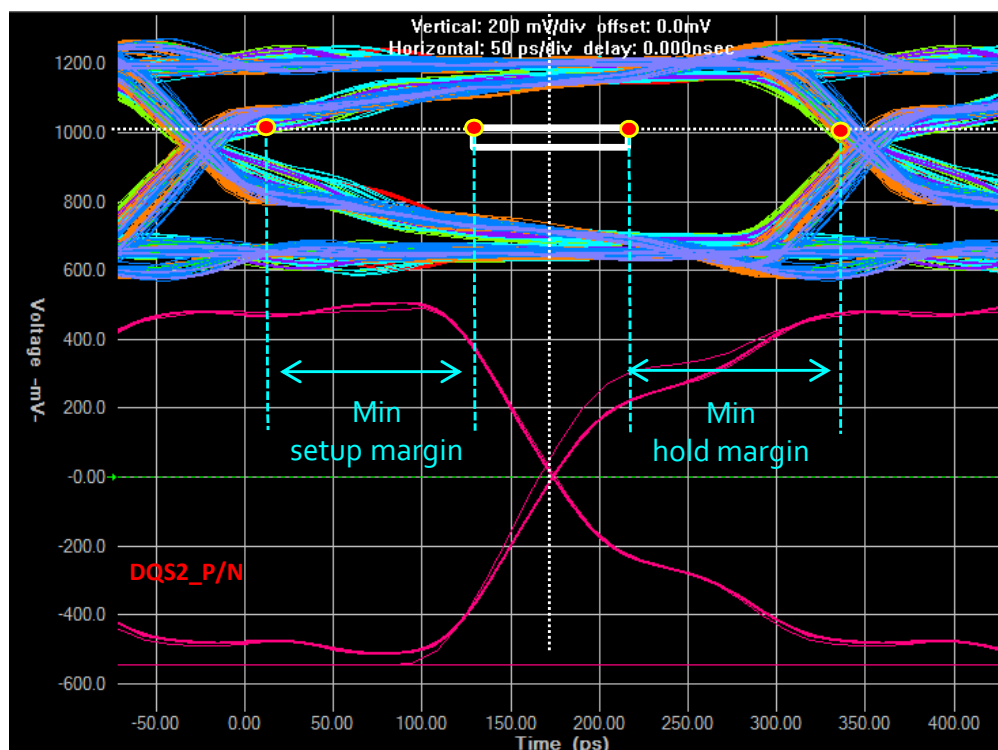


Note :

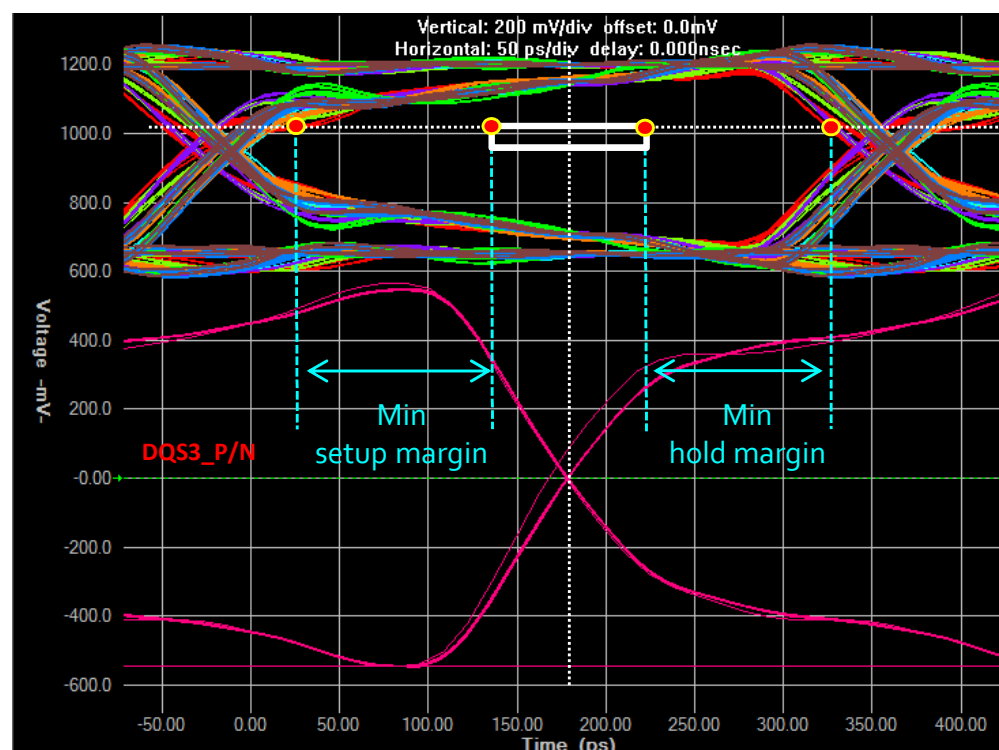
Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

Data Write Simulation Waveform(typ) @DDR U504

DQS2 vs. DQ[16:23], DMASK2



DQS3 vs. DQ[24:31], DMASK3

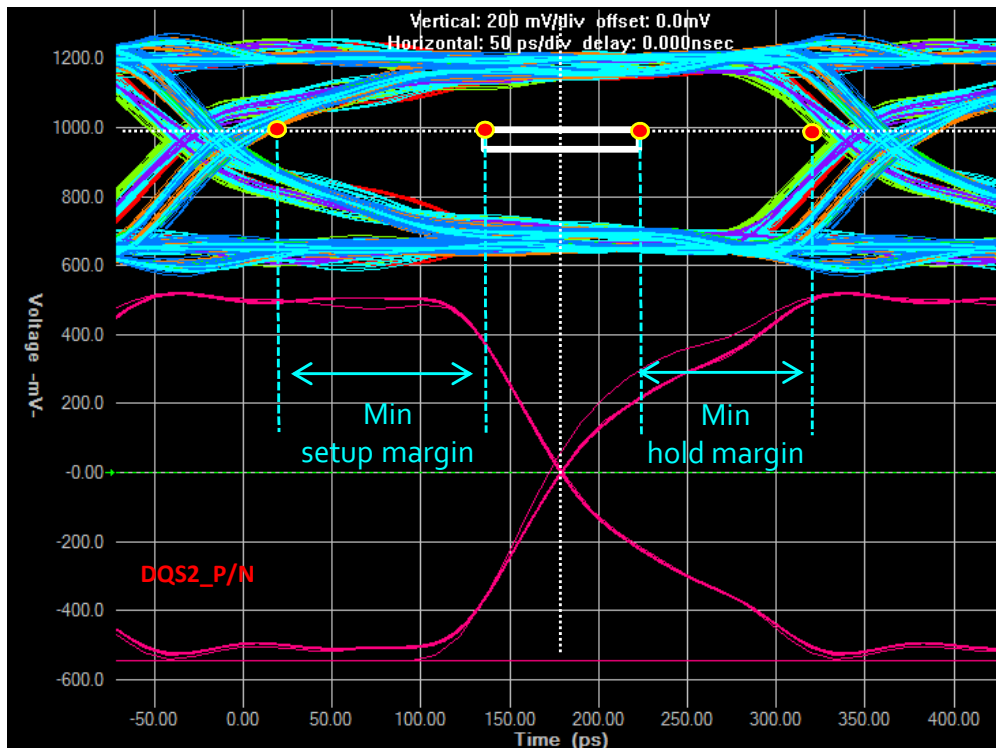


Note :

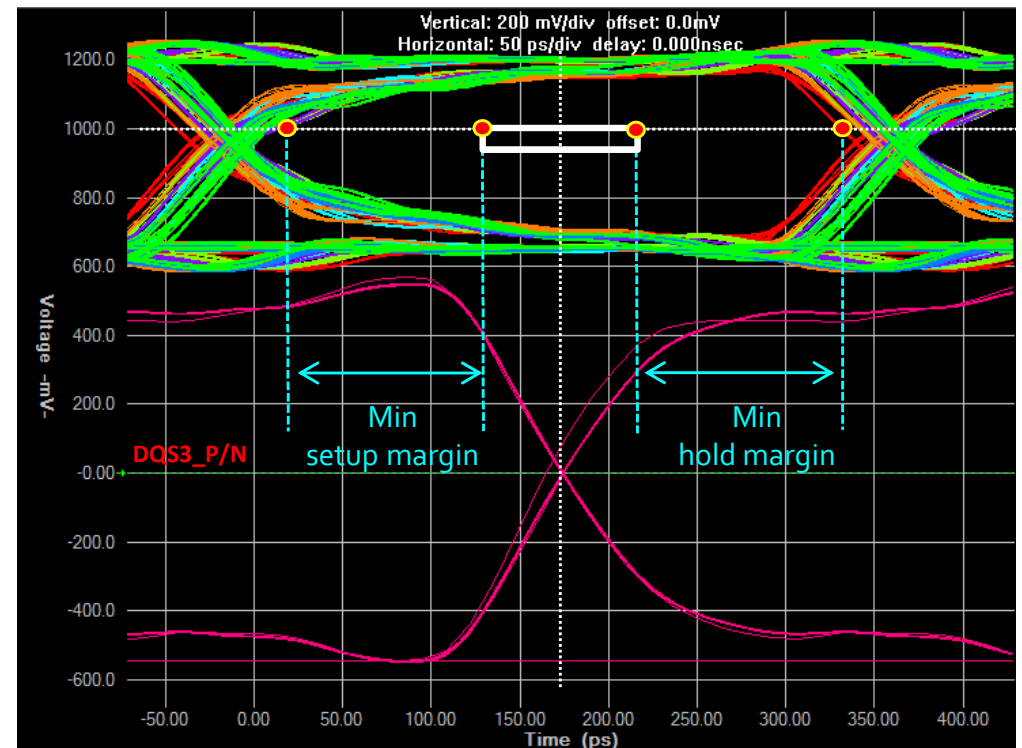
Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

Data Write Simulation Waveform(typ) @DDR U506

DQS2 vs. DQ[16:23], DMASK2



DQS3 vs. DQ[24:31], DMASK3

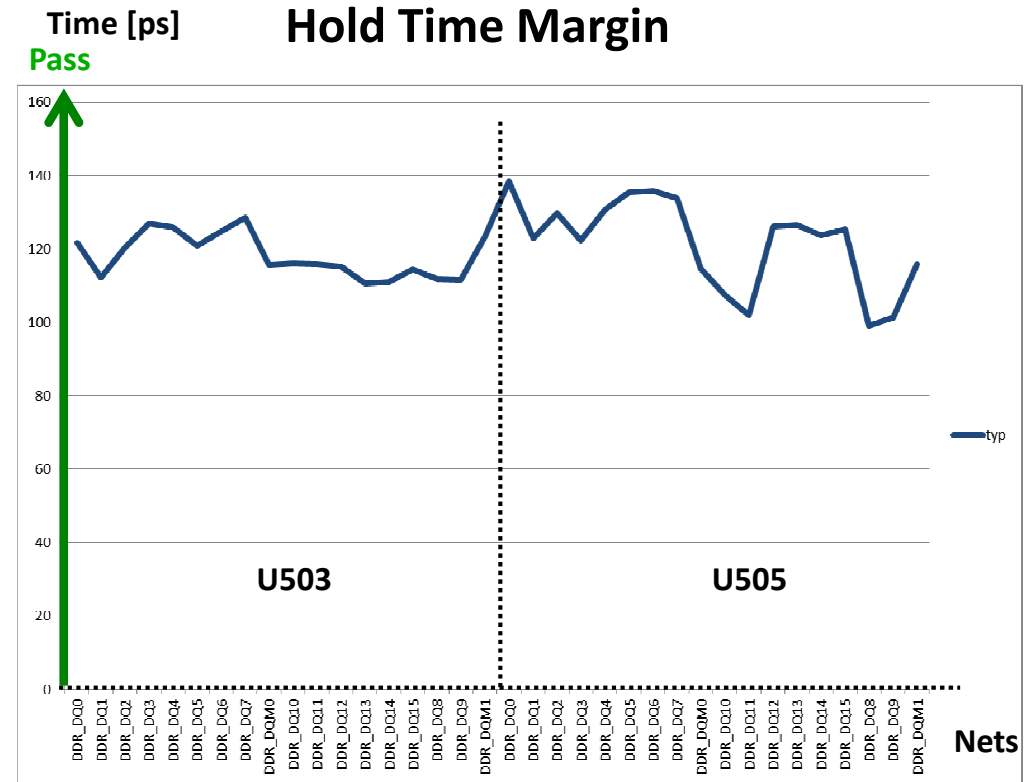
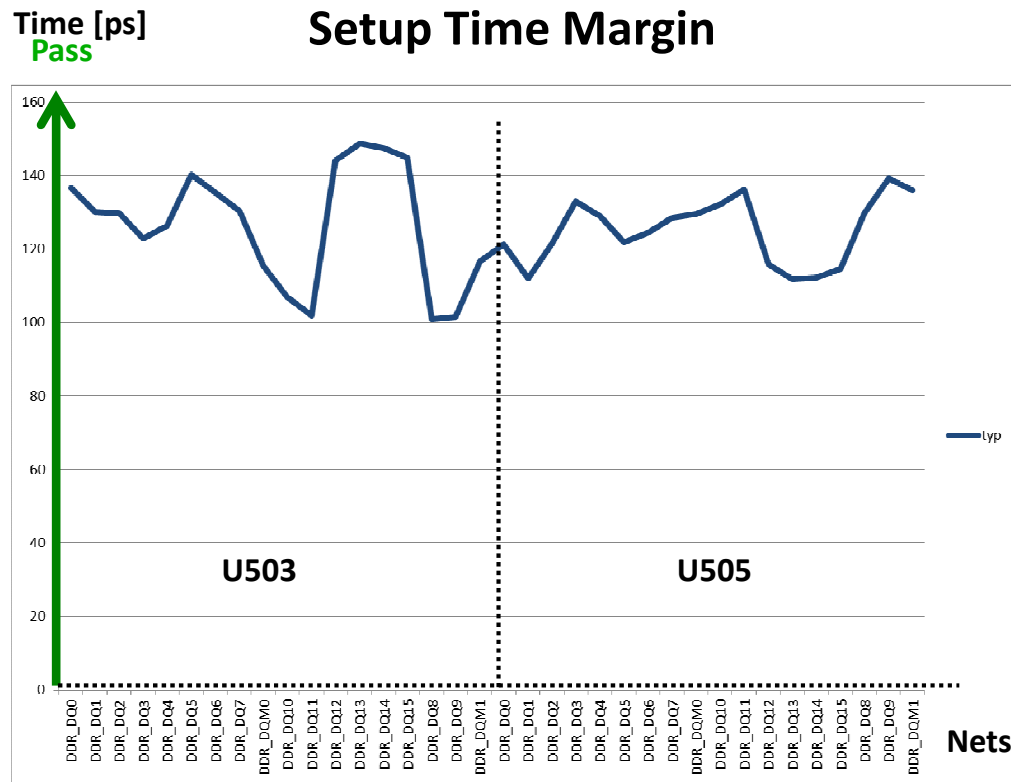


Note :

Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

DQS vs. DQ Write Timing Budget @U503 & U505

Pass

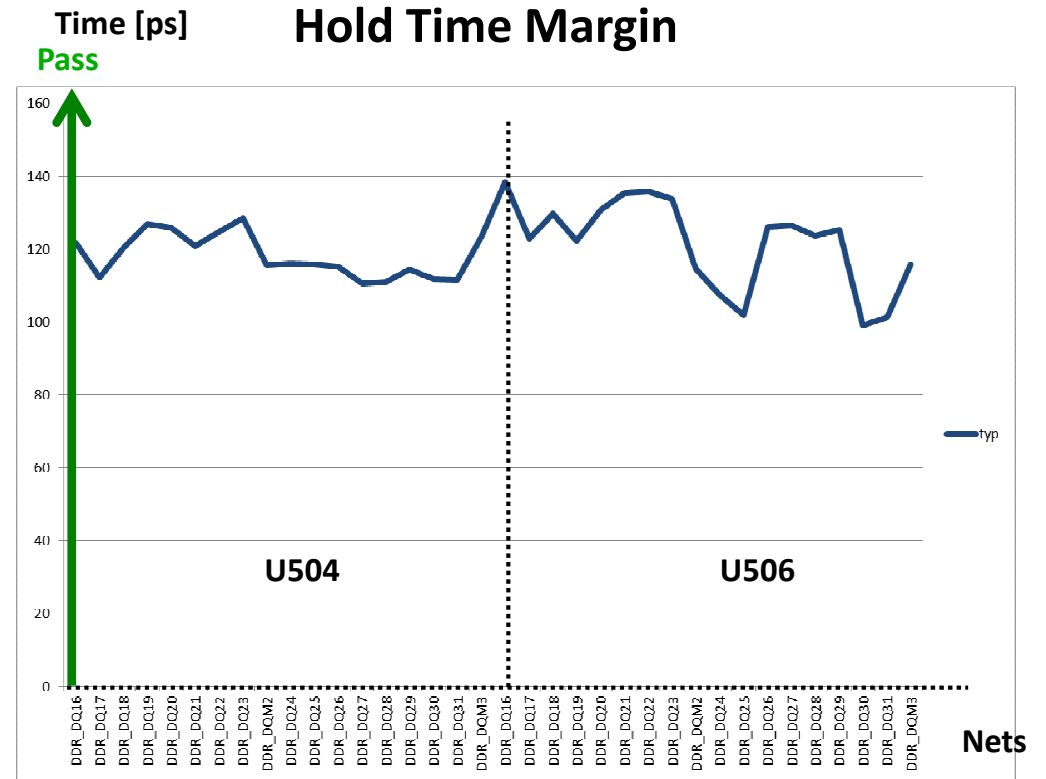
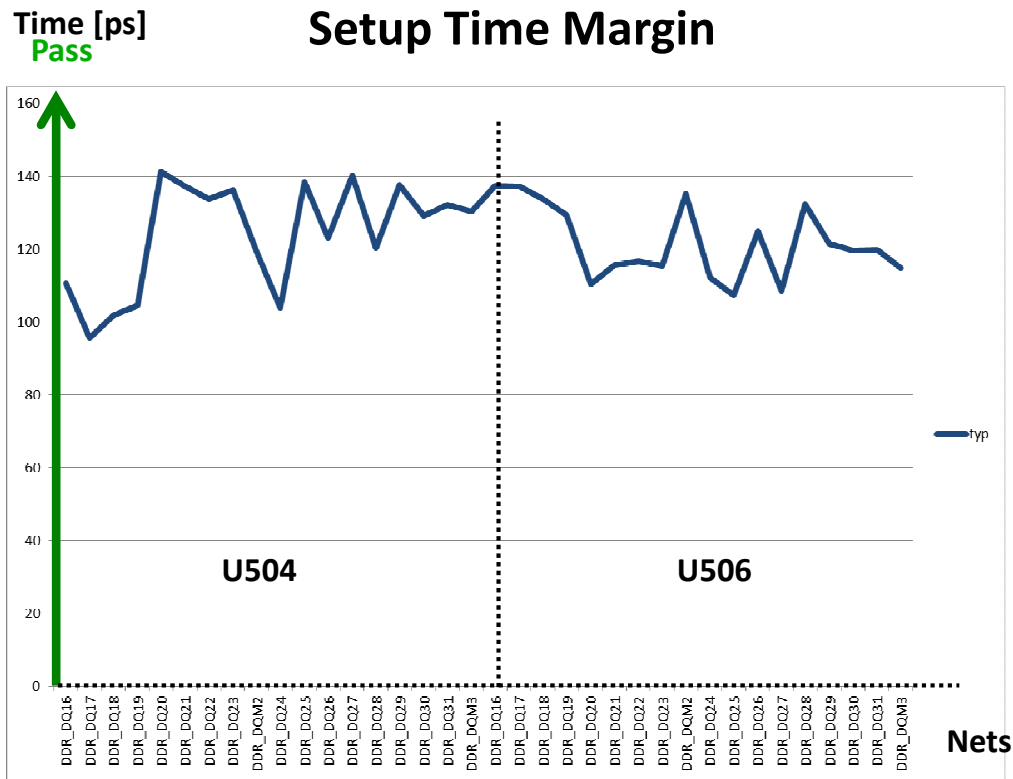


Note :

1. Based on CPU drive strength "mal4drv27_d4_34", and DDR "DQ_ODT_60" on die termination.
2. Both setup/hold time margin should be within specification limit to have enough margin in each nets for pass condition.

DQS vs. DQ Write Timing Budget @U504 & U506

Pass



Note :

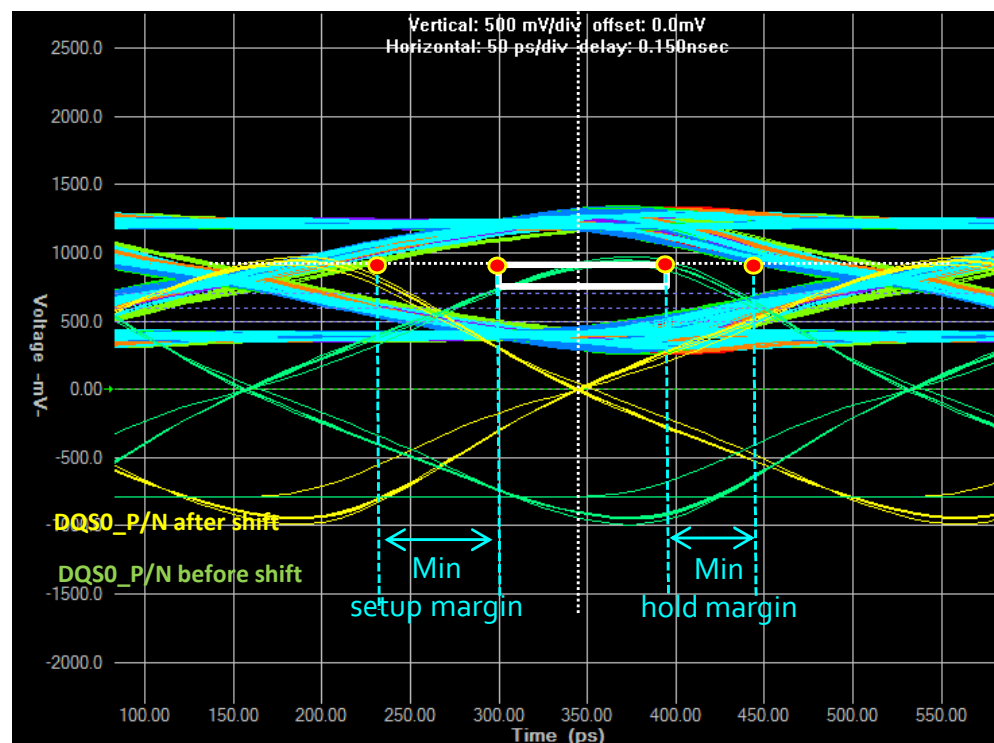
1. Based on CPU drive strength "mal4drv27_d4_34", and DDR "DQ_ODT_60" on die termination.
2. Both setup/hold time margin should be within specification limit to have enough margin in each nets for pass condition.

Post-Layout Simulation

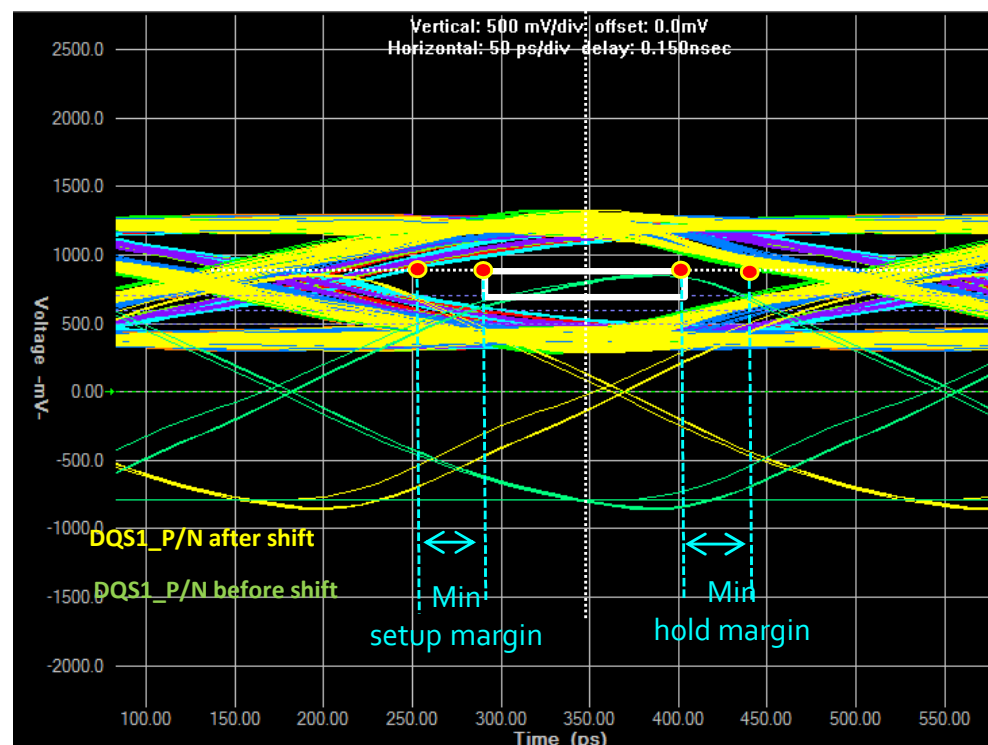
- **CK v.s CA Write**
 - Simulation Waveform & Timing Margin Analysis
- **DQS v.s DQ Write**
 - Simulation Waveform & Timing Margin Analysis
- **DQS v.s DQ Read**
 - Simulation Waveform & Timing Margin Analysis

Data Read Simulation Waveform(typ) @DDR U503

DQS0 vs. DQ[0:7]



DQS1 vs. DQ[8:15]

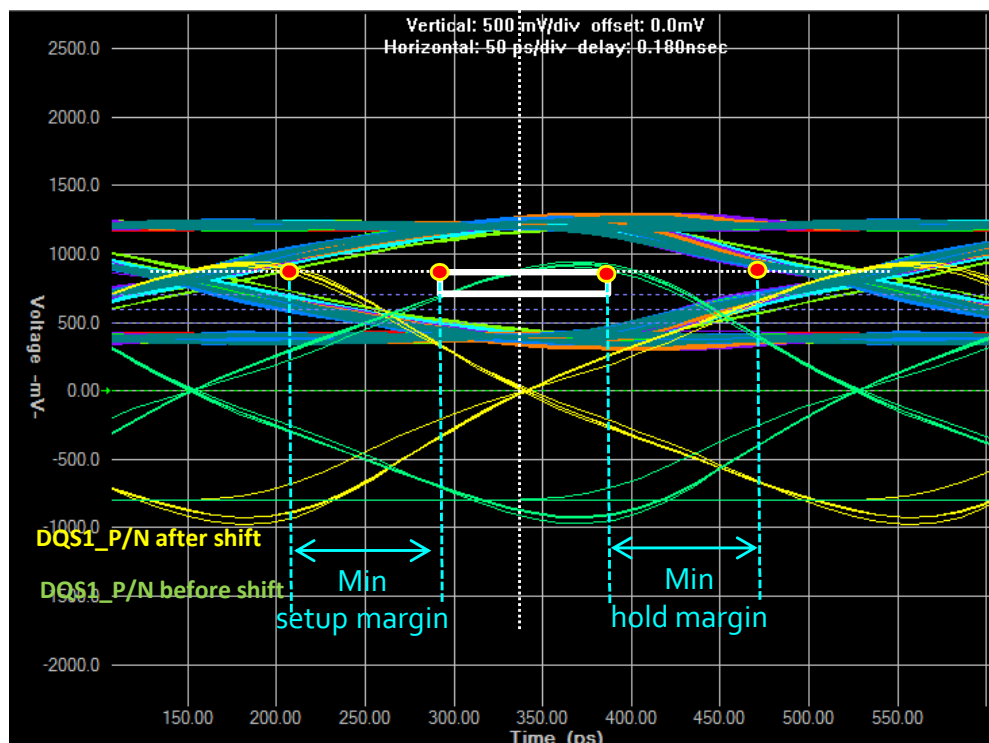


Note :

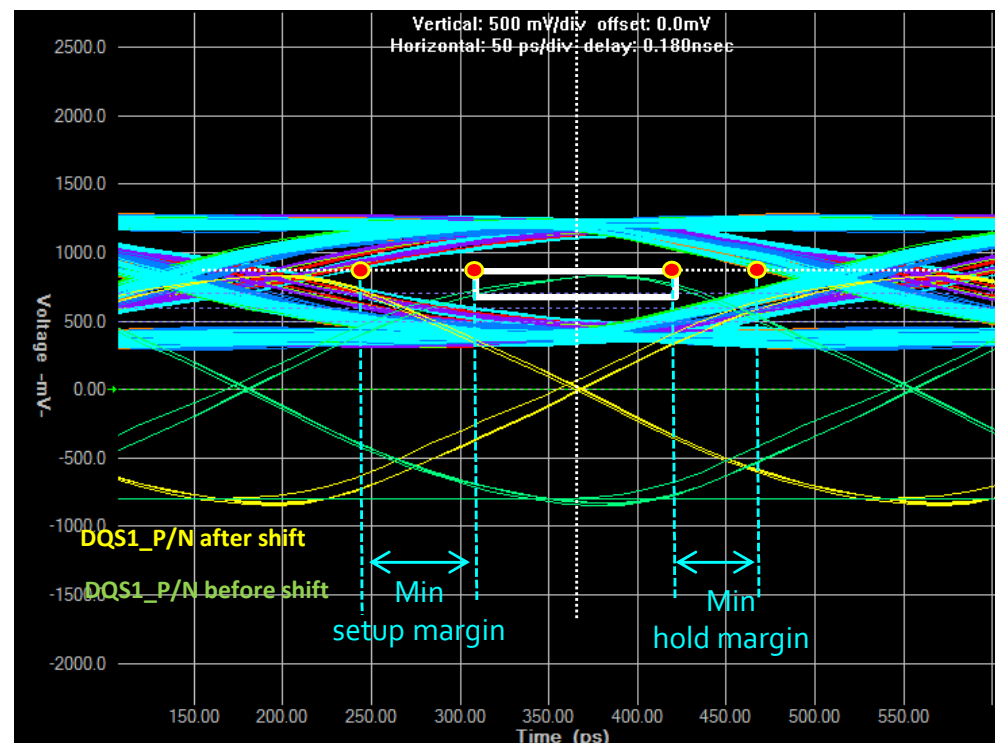
Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

Data Read Simulation Waveform(typ) @DDR U505

DQS0 vs. DQ[0:7]



DQS1 vs. DQ[8:15]

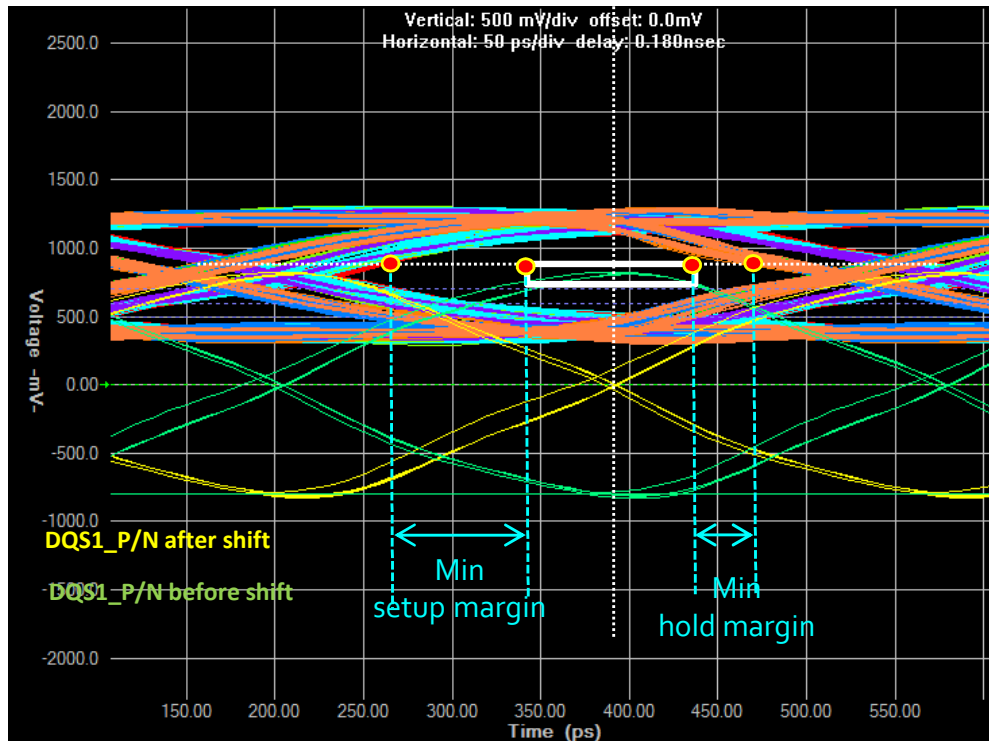


Note :

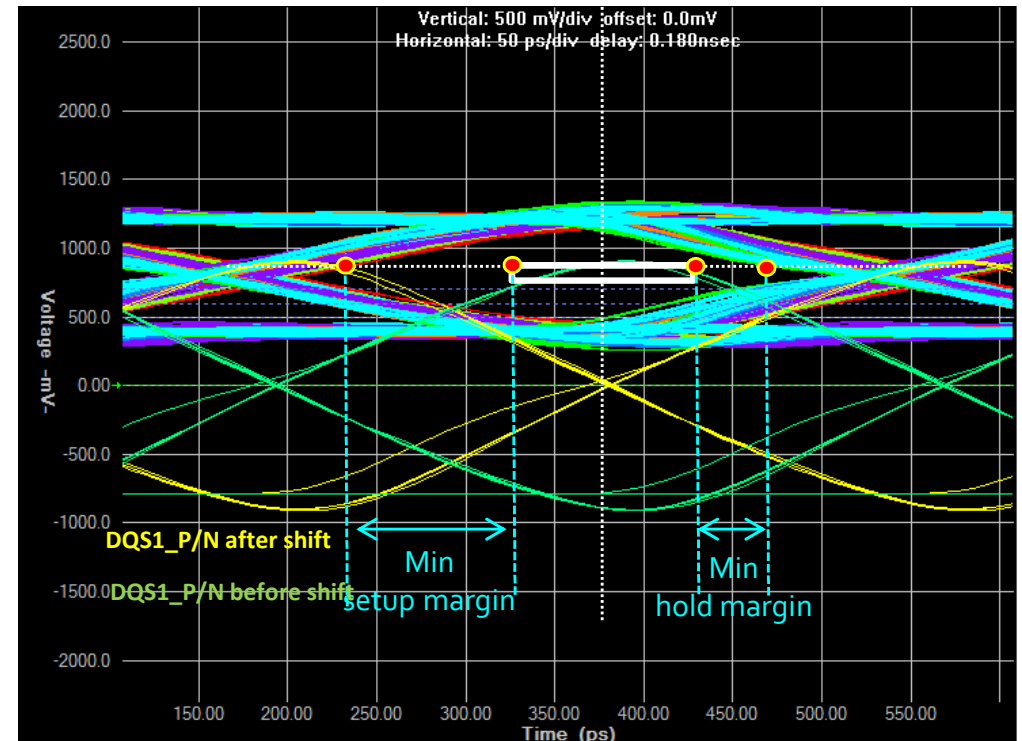
Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

Data Read Simulation Waveform(typ) @DDR U504

DQS0 vs. DQ[0:7]



DQS1 vs. DQ[8:15]

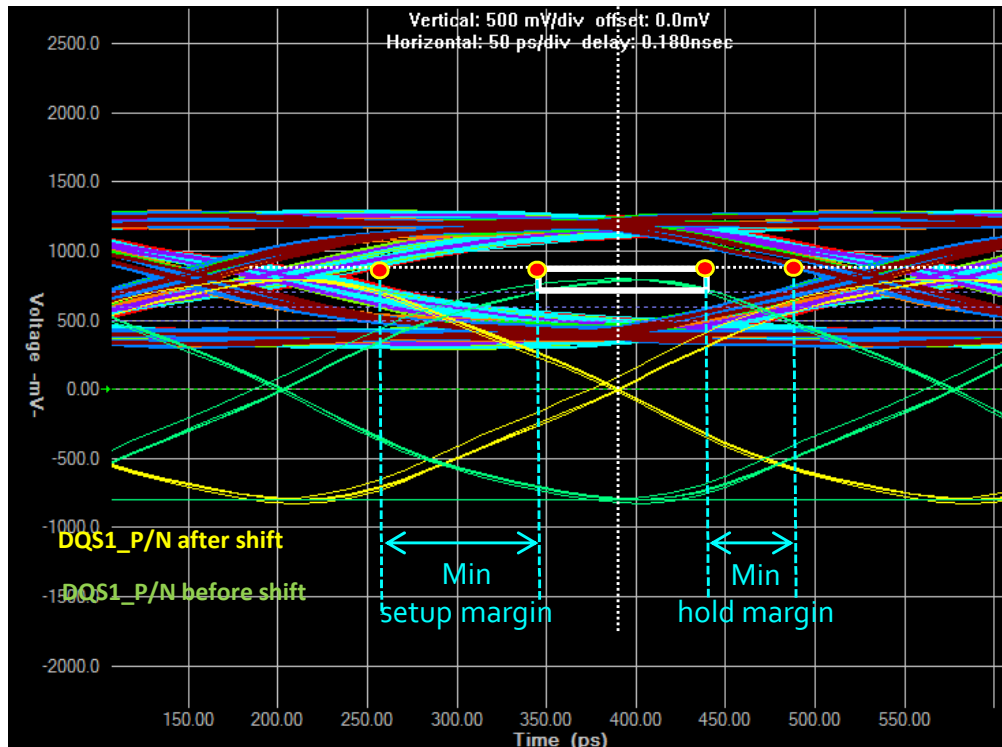


Note :

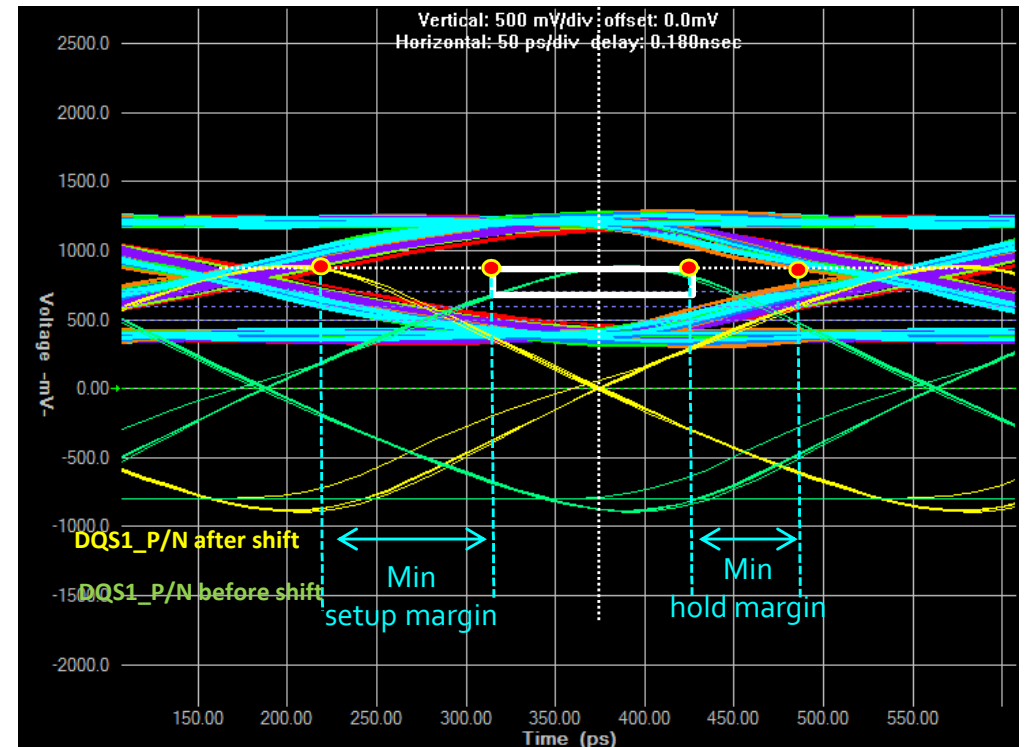
Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

Data Read Simulation Waveform(typ) @DDR U506

DQS0 vs. DQ[0:7]



DQS1 vs. DQ[8:15]

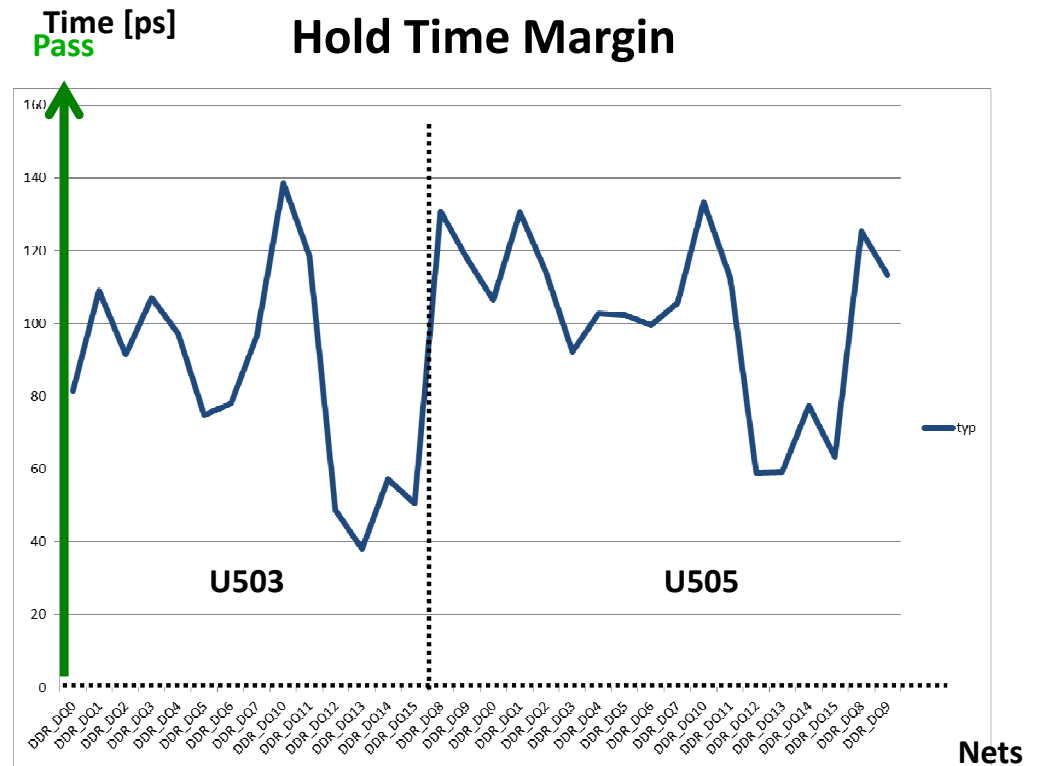
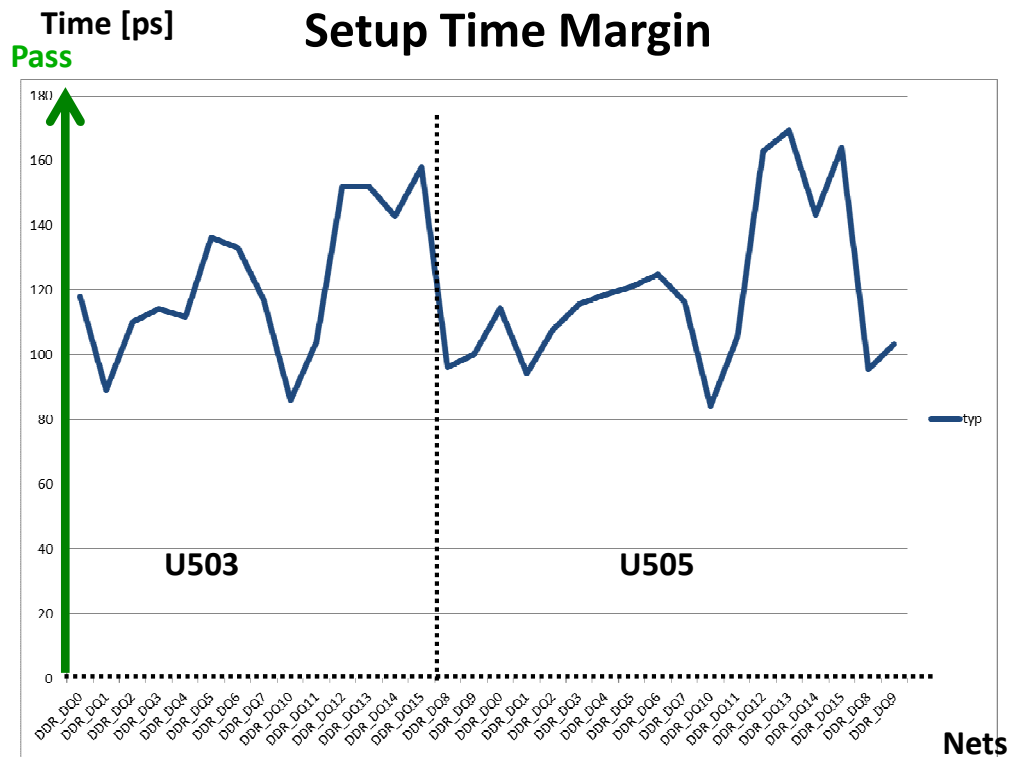


Note :

Data Rx mask voltage and timing total input valid window where V_{DIVW} is centered around V_{cent_DQ} (midpoint) after V_{refDQ} training is completed. These give the margin available at the receiver after taking into account the worst case eye location, the eye-mask requirement, and the amount of output jitter/uncertainty.

DQS vs. DQ Read Timing Budget @U503 & U505

Pass

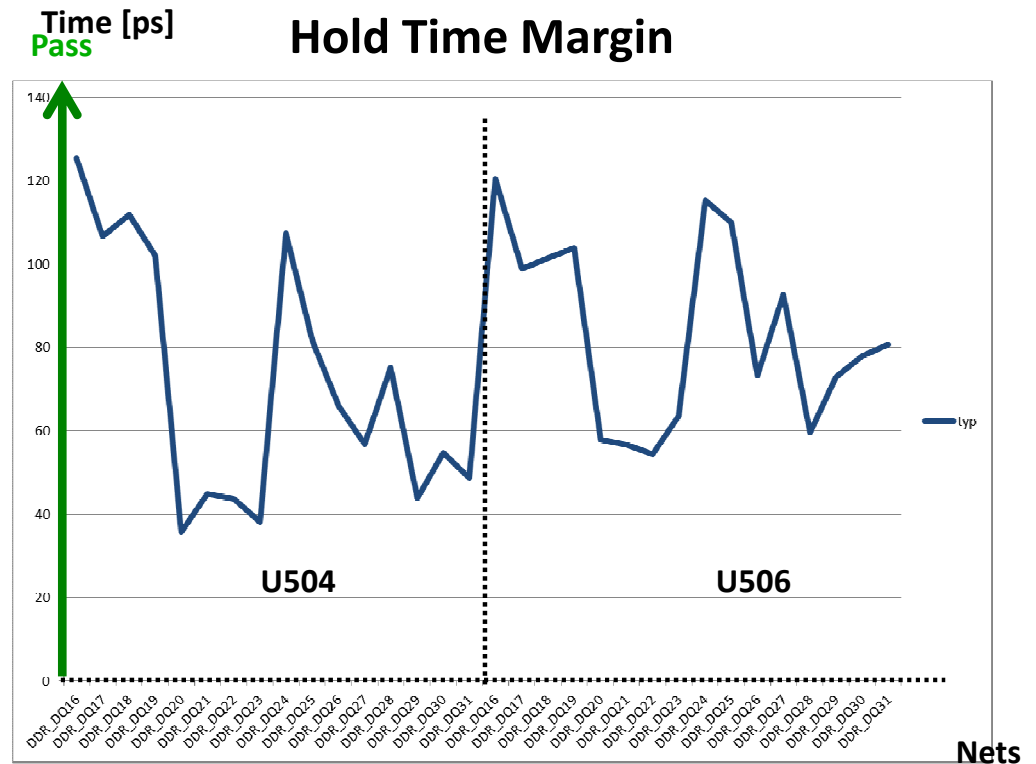
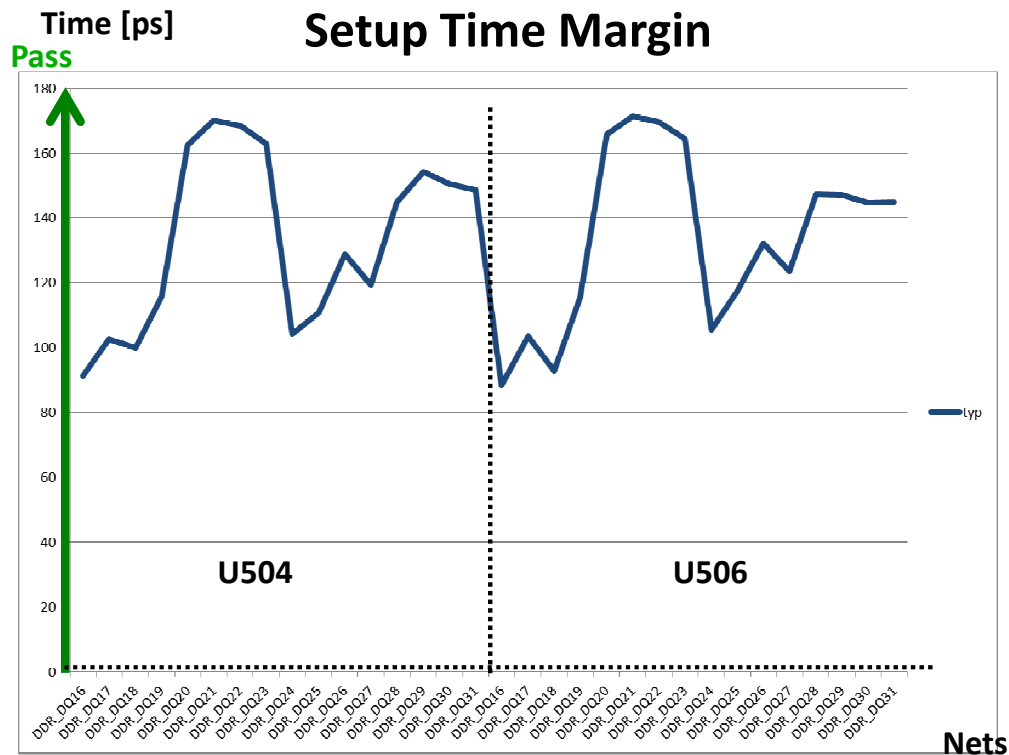


Note :

1. Based on DRAM drive strength "DQ_RON34_ODT_OFF", and CPU "mal4drv27_d4_60" on die termination.
2. All setup/hold time margin should be positive and within specification limit to have enough margin in each nets for pass condition.

DQS vs. DQ Read Timing Budget @U504 & U506

Pass



Note :

1. Based on DRAM drive strength "DQ_RON34_ODT_OFF", and CPU "mal4drv27_d4_60" on die termination.
2. All setup/hold time margin should be positive and within specification limit to have enough margin in each nets for pass condition.

Conclusion



The simulation result :

1. The ADD/CMD timing simulation result show enough budget of time margin for pass condition.
2. The Data simulation result show enough budget of time margin for pass condition.



Summary Table of IC Buffers Selector:

Write Setting(CPU→DRAM)			
Component	Provider	Type	Model
CPU	Qualcomm	CLK	mal4drv20_d4_30
		ADD/CMD	mal4drv20_d4_30
		DQS	mal4drv27_d4_34
		DQ	mal4drv27_d4_34
DRAM	Micron	CLK	CLOCK_PIN
		ADD/CMD	ADDR_PIN
		DQS	DQ_ODT_60
		DQ	DQ_ODT_60
Read Setting(CPU→DRAM)			
CPU	Qualcomm	DQS	mal4drv27_d4_60
		DQ	mal4drv27_d4_60
DRAM	Micron	DQS	DQ_RON34_ODT_OFF
		DQ	DQ_RON34_ODT_OFF