

Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info DPO71604C - 7.6.0 Build 7
 TDSHT3 Version 5.3.1 Build 0

Device Configuration

Device Details HDMI Device
 Clock Frequency(Mhz) 27.0000
 Resolution 480P_60Hz
 Refresh Rate 60Hz

Compliance Summary

Total Tests Supported 9
 Tests Completed 29
 Pass 29
 Fail 0

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.025*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.03*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.03*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.03*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.001*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0.001*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	212.95ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	188.54ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	183.63ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	178.11ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	198.87ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	182.87ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	172.34ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	168.17ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.49%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.68%	Pass
18	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	CK+	2.700V < VL < 2.900V;	2.8750V	Pass
19	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	CK-	2.700V < VL < 2.900V;	2.8700V	Pass
20	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D0+	2.700V < VL < 2.900V;	2.8650V	Pass
21	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D0-	2.700V < VL < 2.900V;	2.8600V	Pass
22	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D1+	2.700V < VL < 2.900V;	2.8450V	Pass
23	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D1-	2.700V < VL < 2.900V;	2.8450V	Pass
24	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D2+	2.700V < VL < 2.900V;	2.8450V	Pass
25	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D2-	2.700V < VL < 2.900V;	2.8450V	Pass
26	7-7 : Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.003*Tbit	Pass
27	7-7 : Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.0*Tbit	Pass
28	7-7 : Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.0*Tbit	Pass
29	7-7 : Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.003*Tbit	Pass

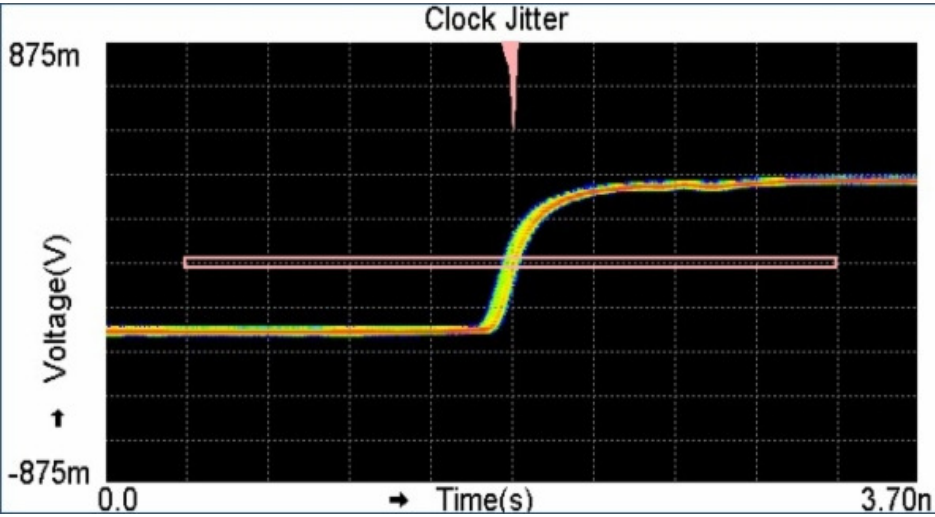
Detailed Results

7-9 : Source Clock Jitter : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Result
Clock Jitter < 0.25*Tbit;	0.025*Tbit	3.7037ns	540.64mV	0.22*Tbit	50.000M	Pass

Waveform/Plot



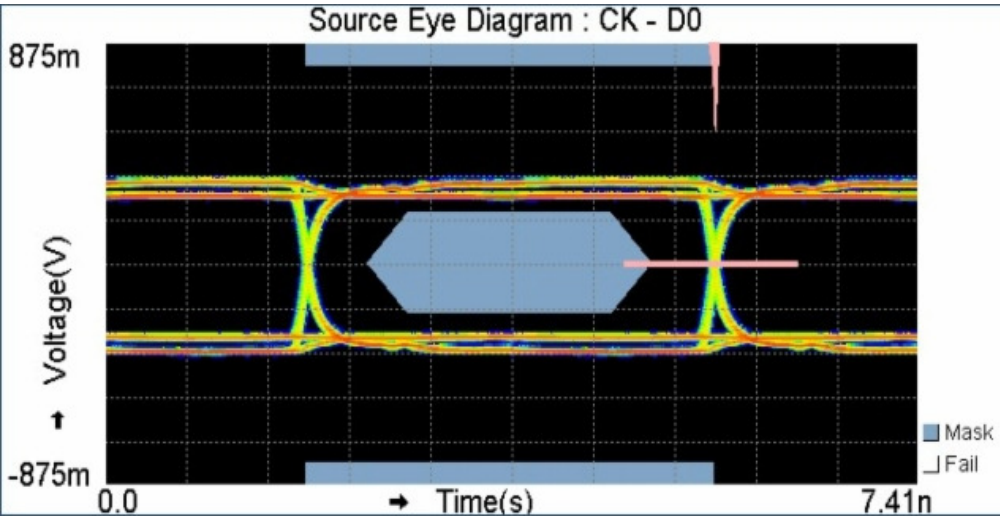
Results	
Result	PASS
Pk-Pk	93.3ps
Vswing	540.64mV
Tbit	3.7037ns

7-10 : Source Eye Diagram : CK - D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.03*Tbit	3.7037ns	555.00mV	269.1m*Tbit	50.000M	0	Pass

Waveform/Plot



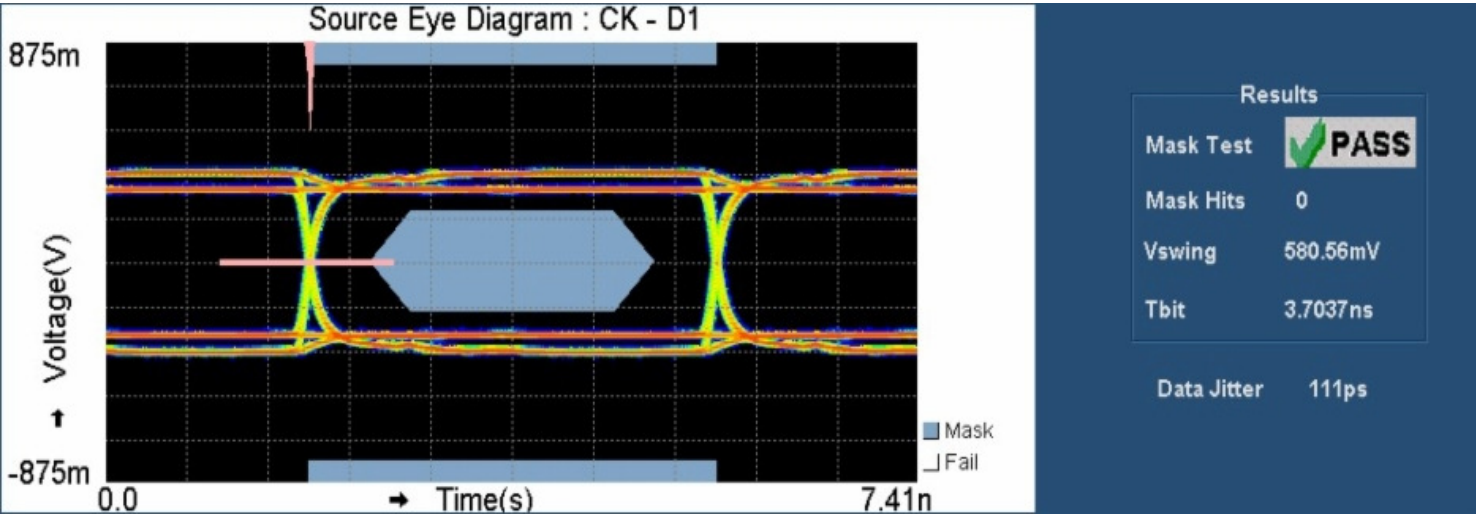
Results	
Mask Test	PASS
Mask Hits	0
Vswing	555.00mV
Tbit	3.7037ns
Data Jitter	115ps

7-10 : Source Eye Diagram : CK - D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.03*Tbit	3.7037ns	580.56mV	270.1m*Tbit	50.000M	0	Pass

Waveform/Plot

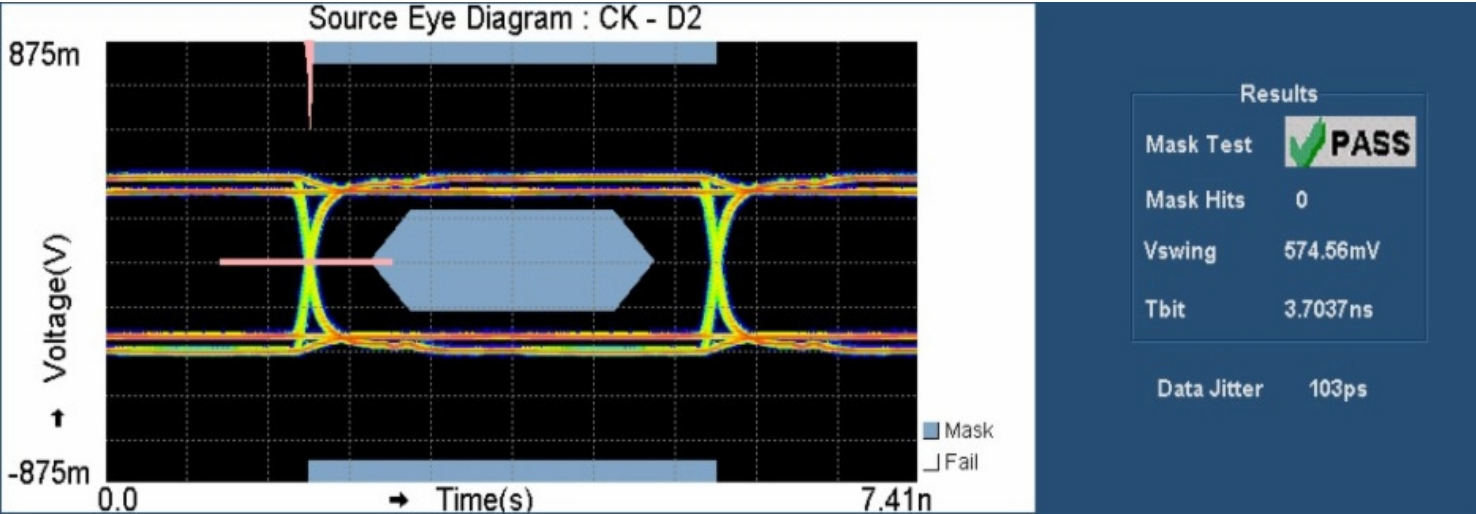


7-10 : Source Eye Diagram : CK - D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.03*Tbit	3.7037ns	574.56mV	272.1m*Tbit	50.000M	0	Pass

Waveform/Plot



7-6 : Source Inter-Pair Skew : D0 - D1

Results

Spec Range	Meas Value	Tbit	Vs(D0 - D1)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.001*TPixel	3.7037ns	= 555.00mV, Vs = 580.56mV	24.881p	31.722p	27.840p	Pass

7-6 : Source Inter-Pair Skew : D1 - D2

Results

Spec Range	Meas Value	Tbit	Vs(D1 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0*TPixel	3.7037ns	= 580.56mV, Vs = 574.56mV	1.0714p	5.2857p	2.3897p	Pass

7-6 : Source Inter-Pair Skew : D2 - D0

Results

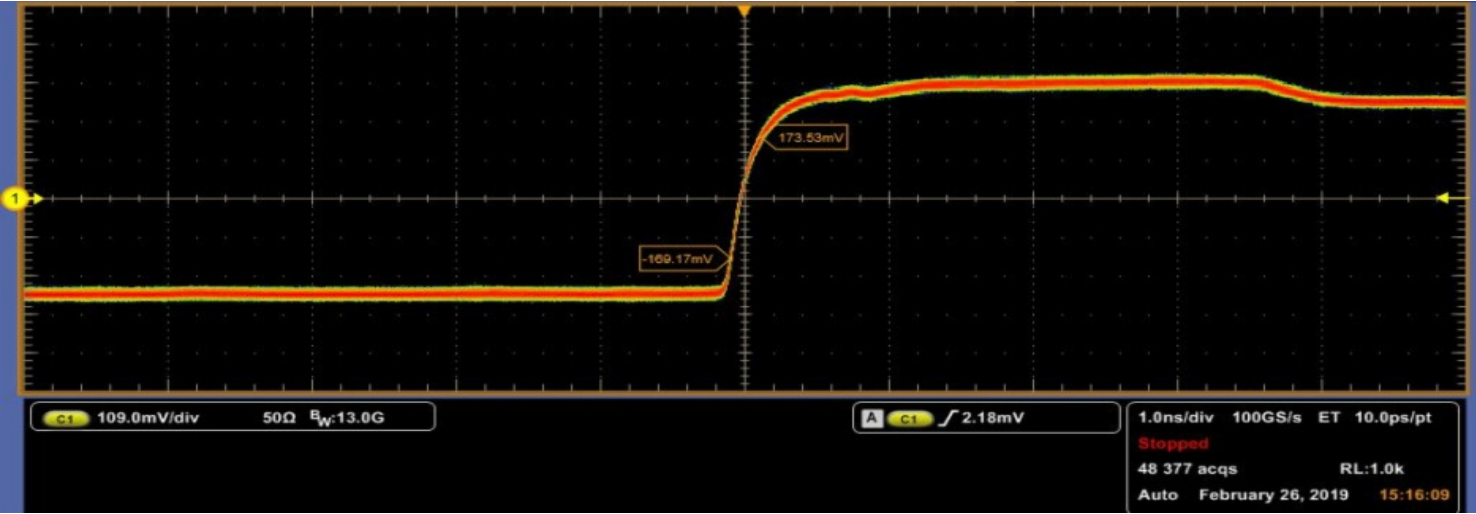
Spec Range	Meas Value	Tbit	Vs(D2 - D0)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.001*TPixel	3.7037ns	= 574.56mV, Vs = 555.00mV	26.762p	33.260p	30.230p	Pass

7-4 : Source Rise Time : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	212.95ps	3.7037ns	571.16mV	138.0ps	Pass

Waveform/Plot

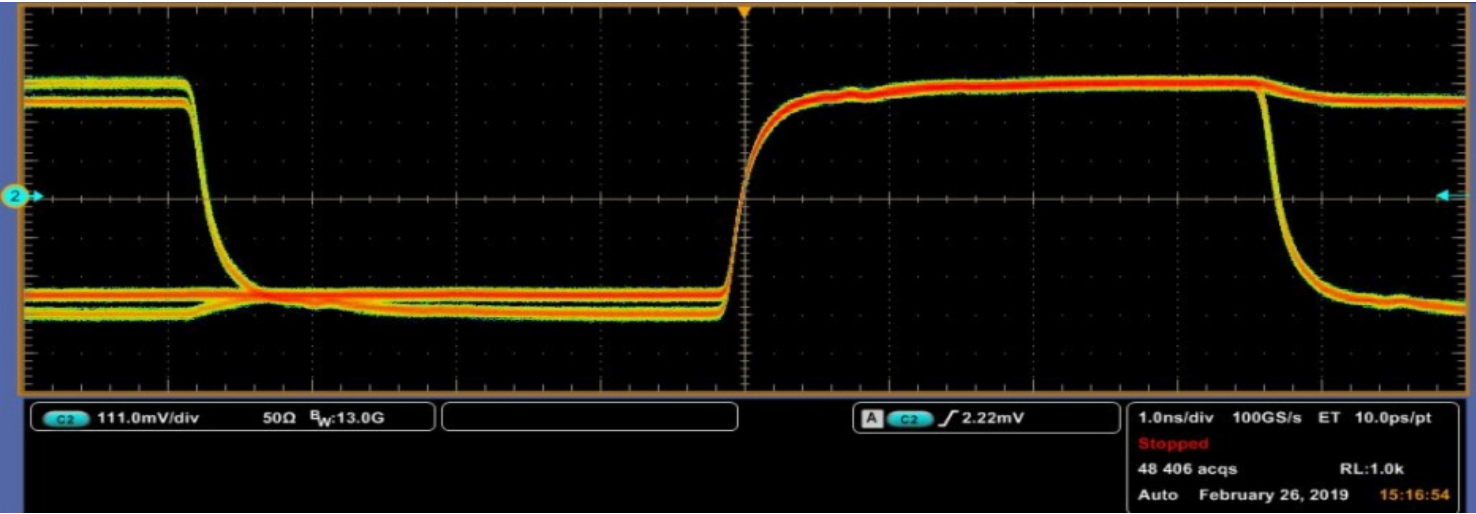


7-4 : Source Rise Time : D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	188.54ps	3.7037ns	559.44mV	113.5ps	Pass

Waveform/Plot

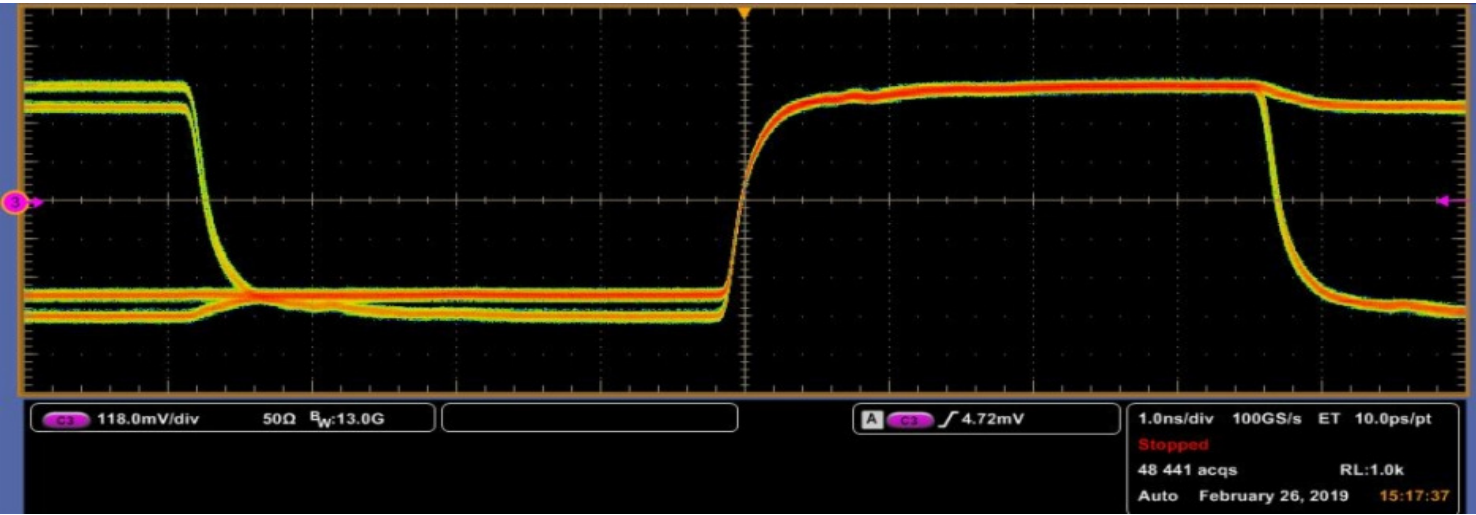


7-4 : Source Rise Time : D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	183.63ps	3.7037ns	580.56mV	108.6ps	Pass

Waveform/Plot

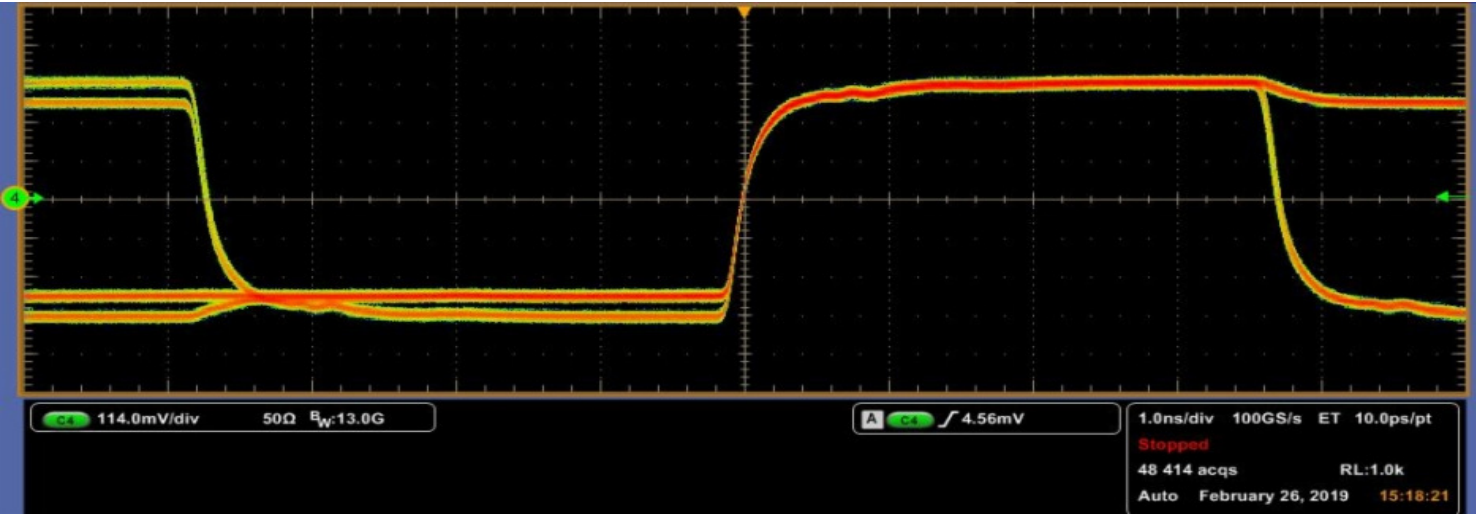


▶ 7-4 : Source Rise Time : D2

▶ Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	178.11ps	3.7037ns	574.56mV	103.1ps	Pass

▶ Waveform/Plot

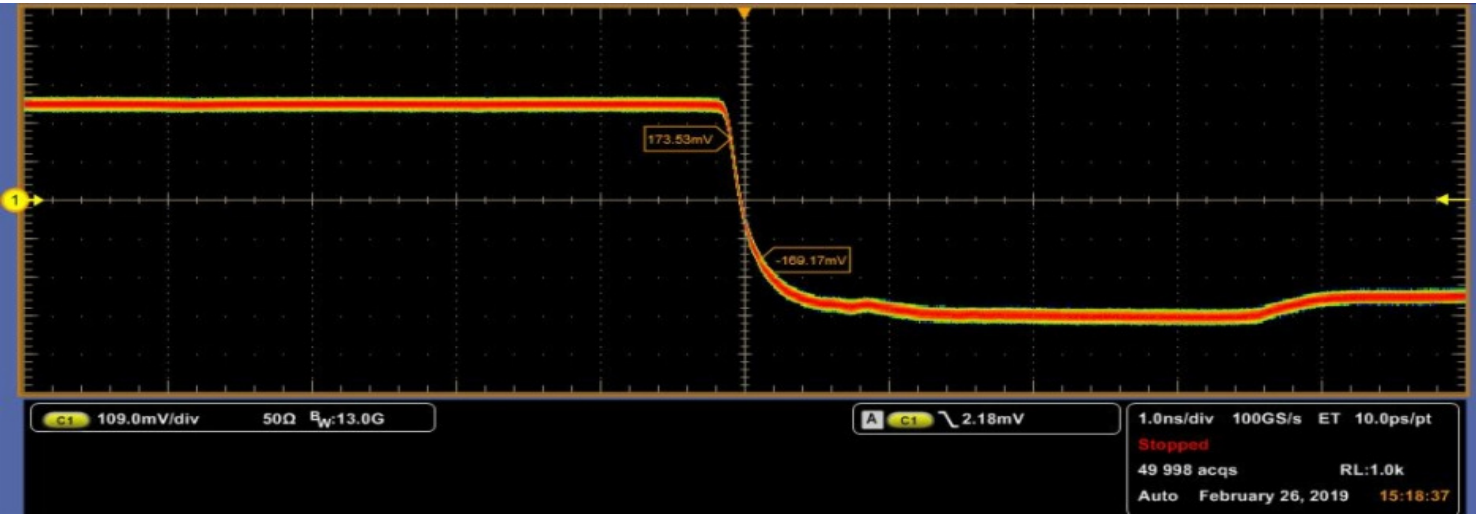


▶ 7-4 : Source Fall Time : CK

▶ Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	198.87ps	3.7037ns	571.16mV	123.9ps	Pass

▶ Waveform/Plot

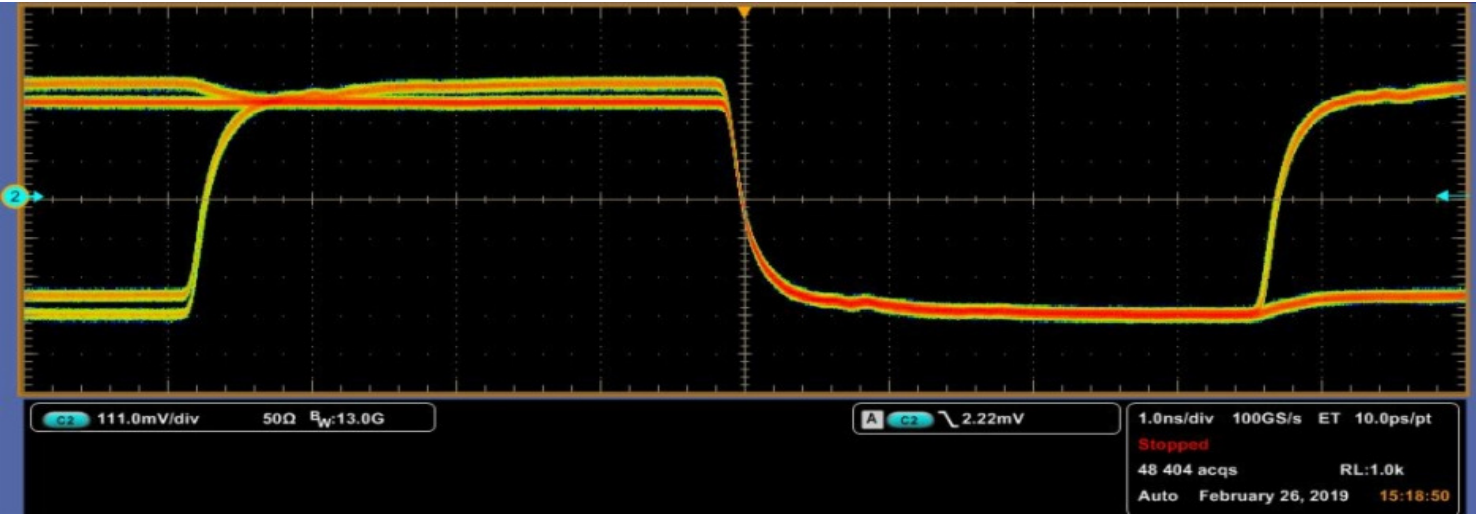


▶ 7-4 : Source Fall Time : D0

▶ Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	182.87ps	3.7037ns	559.44mV	107.9ps	Pass

▶ Waveform/Plot

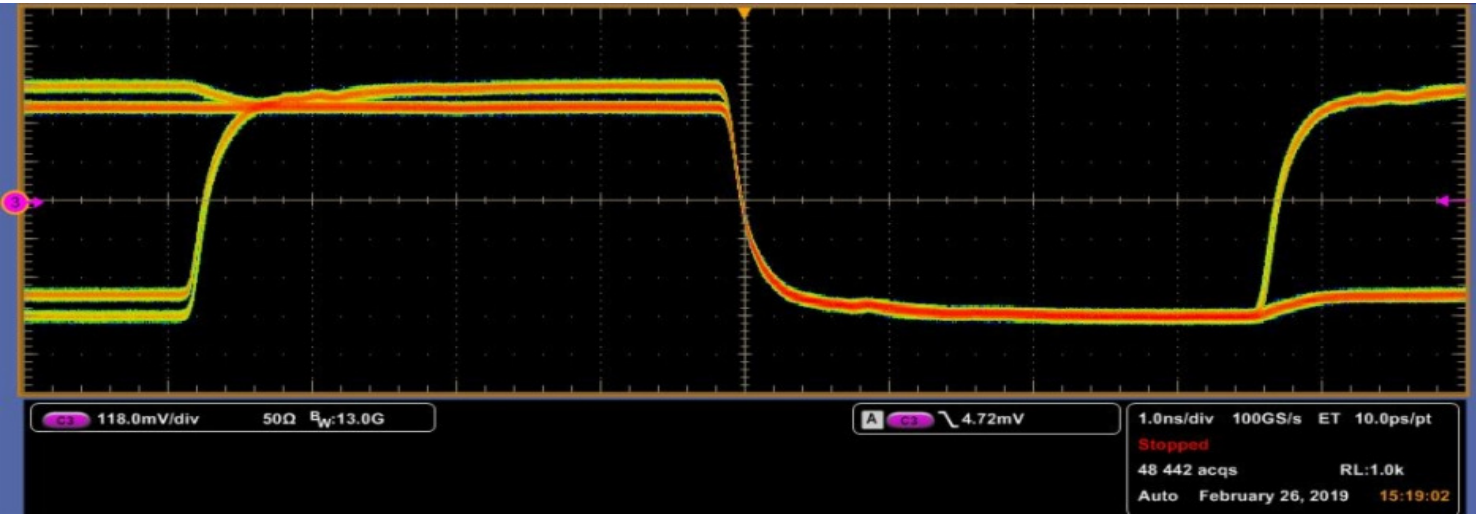


▶ 7-4 : Source Fall Time : D1

▶ Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	172.34ps	3.7037ns	580.56mV	97.34ps	Pass

▶ Waveform/Plot

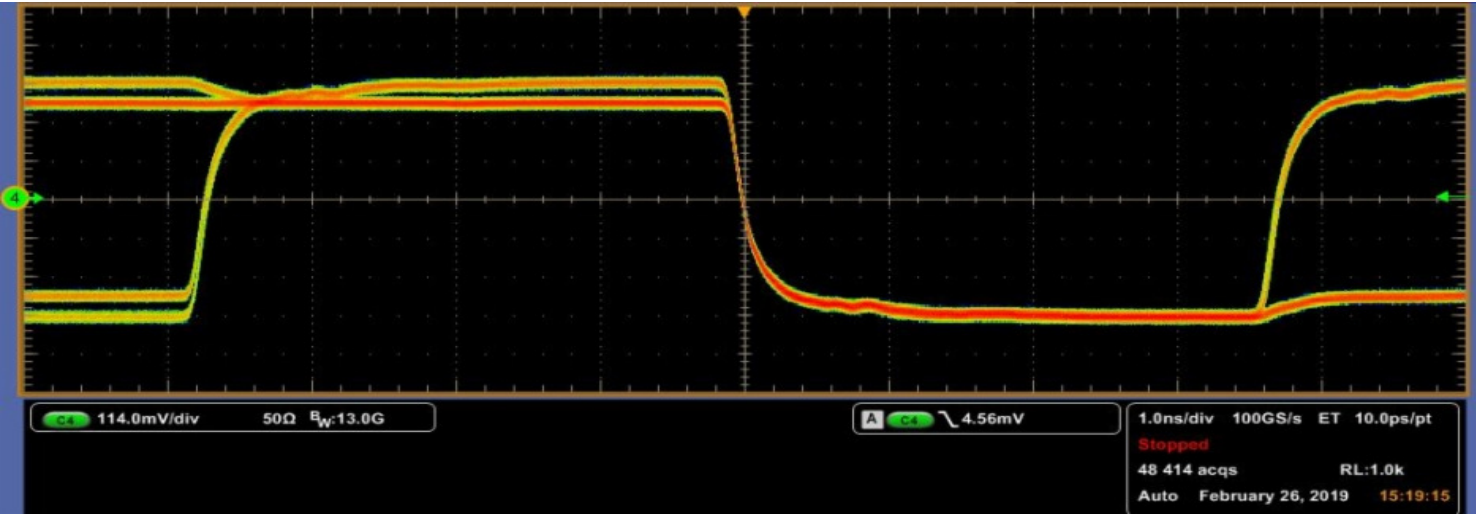


▶ 7-4 : Source Fall Time : D2

▶ Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	168.17ps	3.7037ns	574.56mV	93.17ps	Pass

▶ Waveform/Plot



▶ 7-8 : Max Duty Cycle : CK

▶ Results

Spec Range	Meas Value	Tbit	Margin	Result
Max Duty Cycle < 60.0%;	50.49%	3.7037ns	9.51%	Pass

▶ Waveform/Plot



▶ 7-8 : Min Duty Cycle : CK

▶ Results

Spec Range	Meas Value	Tbit	Margin	Result
40.0% < Min Duty Cycle;	49.68%	3.7037ns	9.68%	Pass

▶ Waveform/Plot



▶ 7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : CK+

▶ Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8750V	25.00mV	175.0mV	Pass

▶ Waveform/Plot



▶ 7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : CK-

▶ Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8700V	30.00mV	170.0mV	Pass

▶ Waveform/Plot

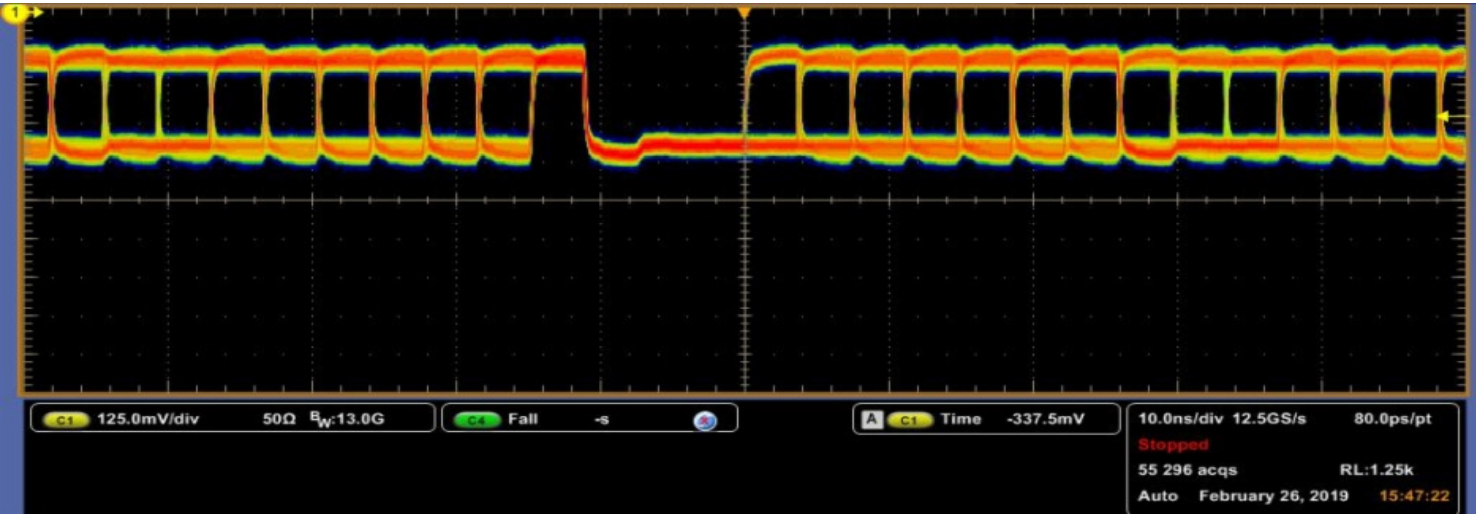


▶ 7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D0+

▶ Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8650V	35.00mV	165.0mV	Pass

▶ Waveform/Plot

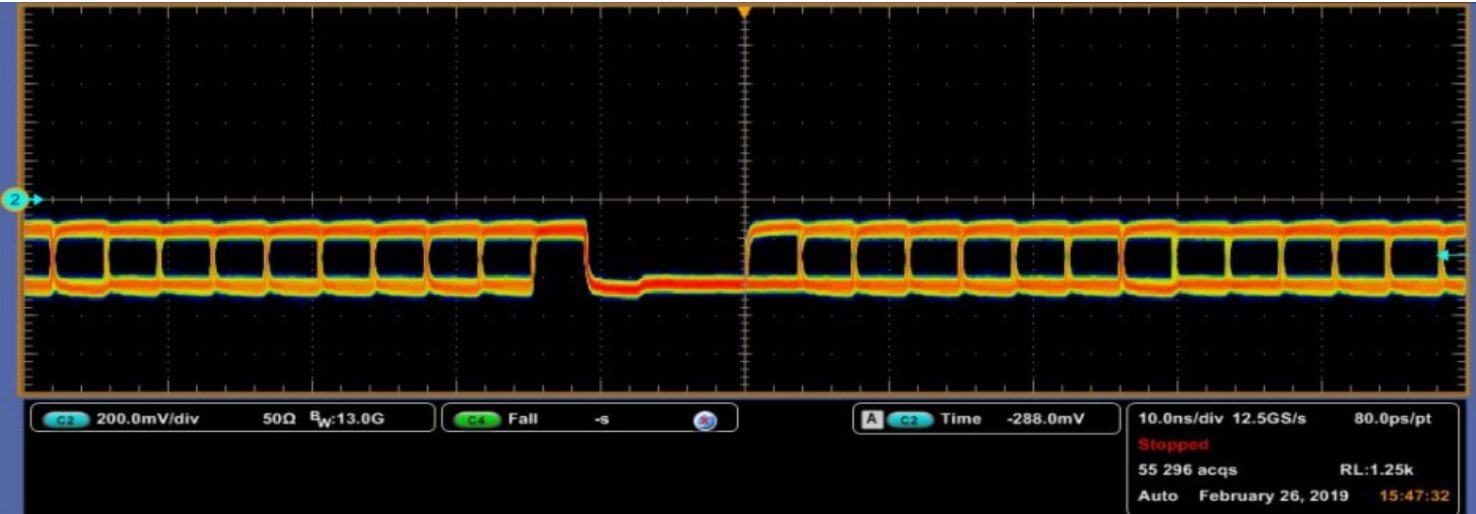


7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D0-

Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8600V	40.00mV	160.0mV	Pass

Waveform/Plot

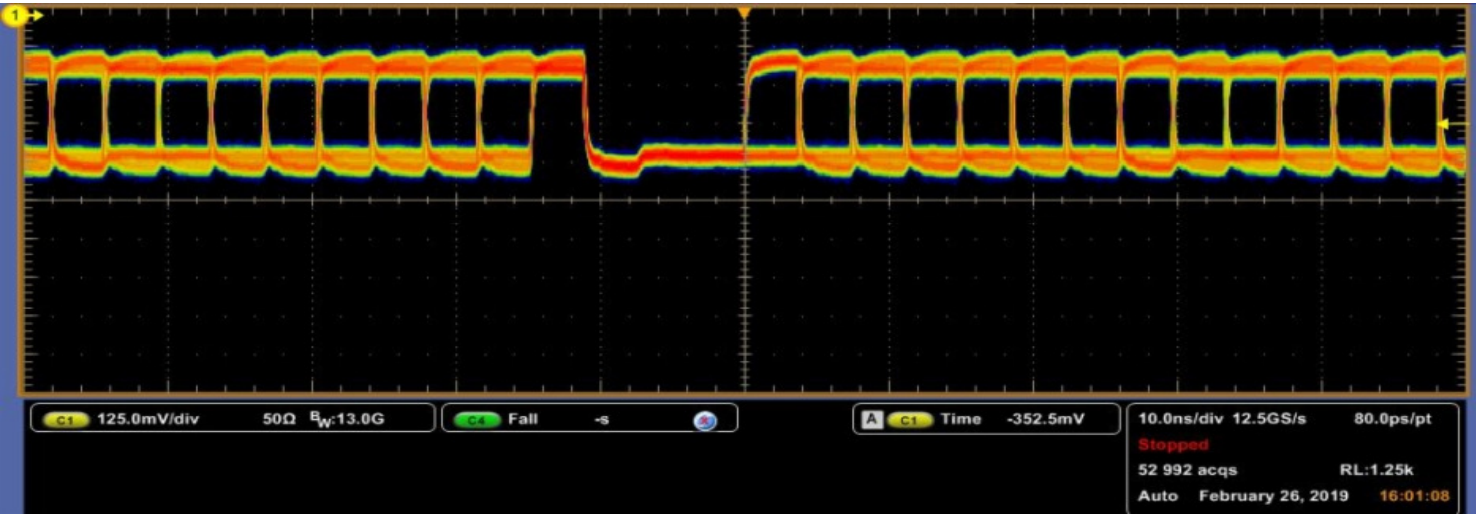


7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D1+

Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8450V	55.00mV	145.0mV	Pass

Waveform/Plot

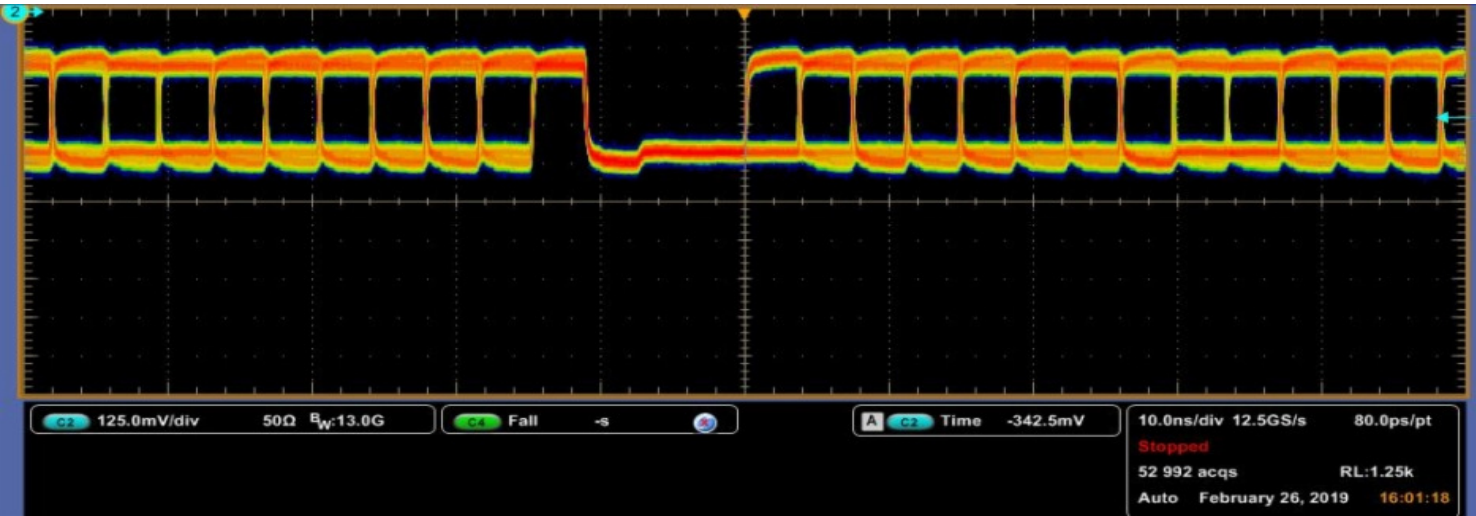


▶ 7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D1-

▶ Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8450V	55.00mV	145.0mV	Pass

▶ Waveform/Plot

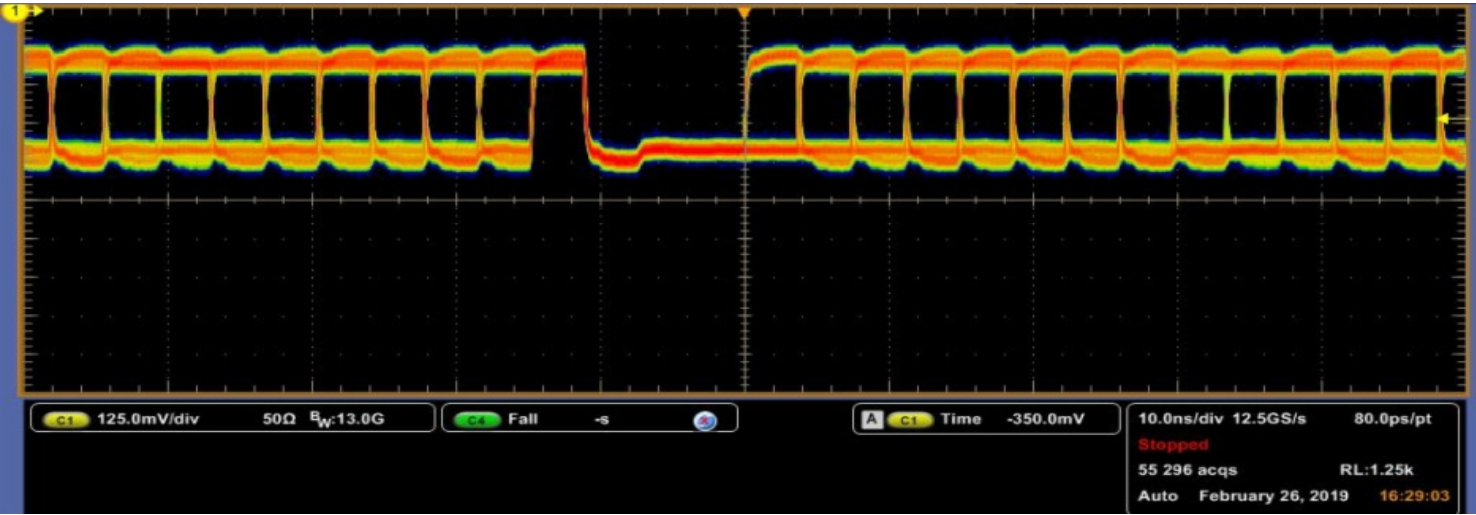


▶ 7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D2+

▶ Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8450V	55.00mV	145.0mV	Pass

▶ Waveform/Plot

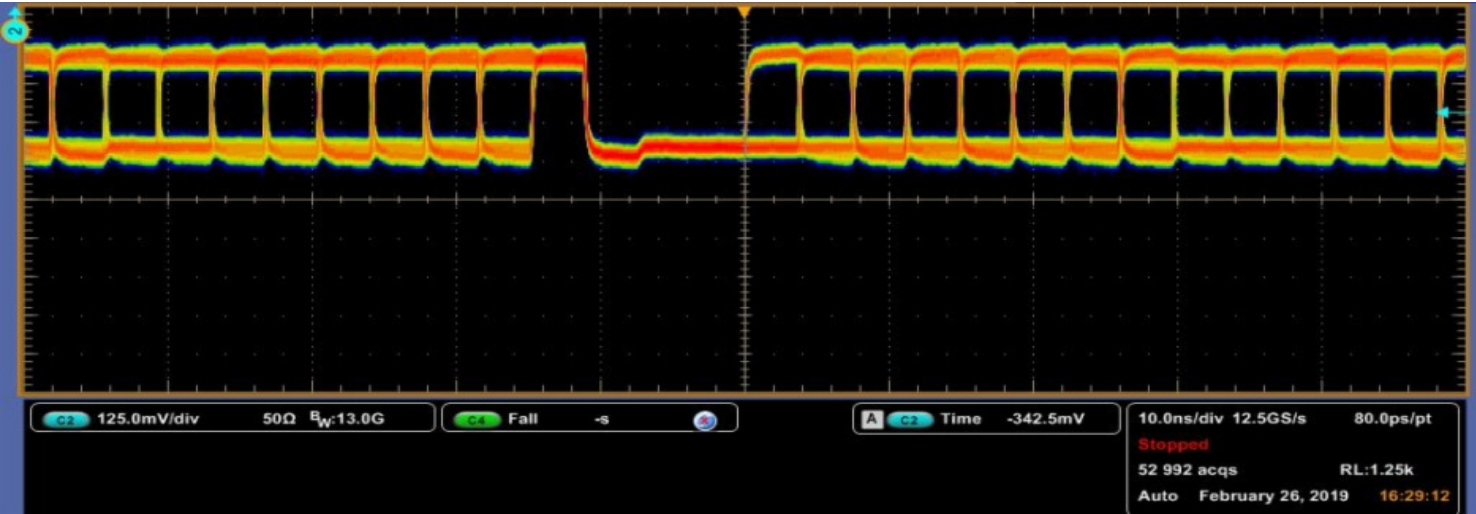


▶ 7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D2-

▶ Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8450V	55.00mV	145.0mV	Pass

▶ Waveform/Plot

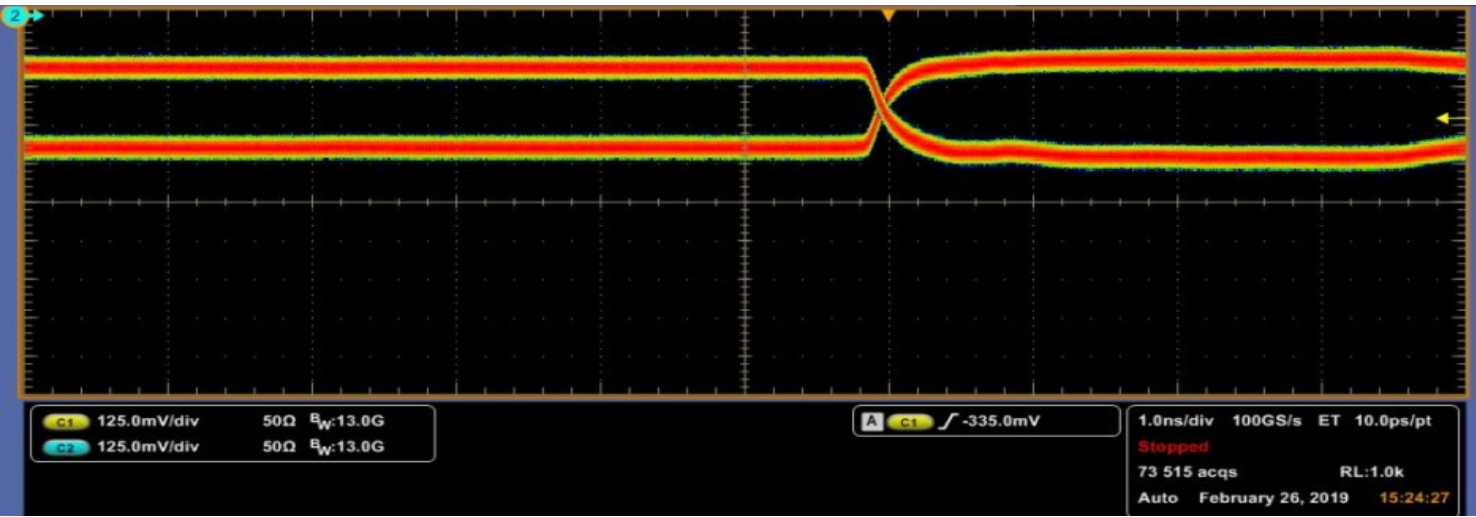


▶ 7-7 : Source Intra-Pair Skew : CK

▶ Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.003*Tbit	3.7037ns	0.15*Tbit	Pass

▶ Waveform/Plot

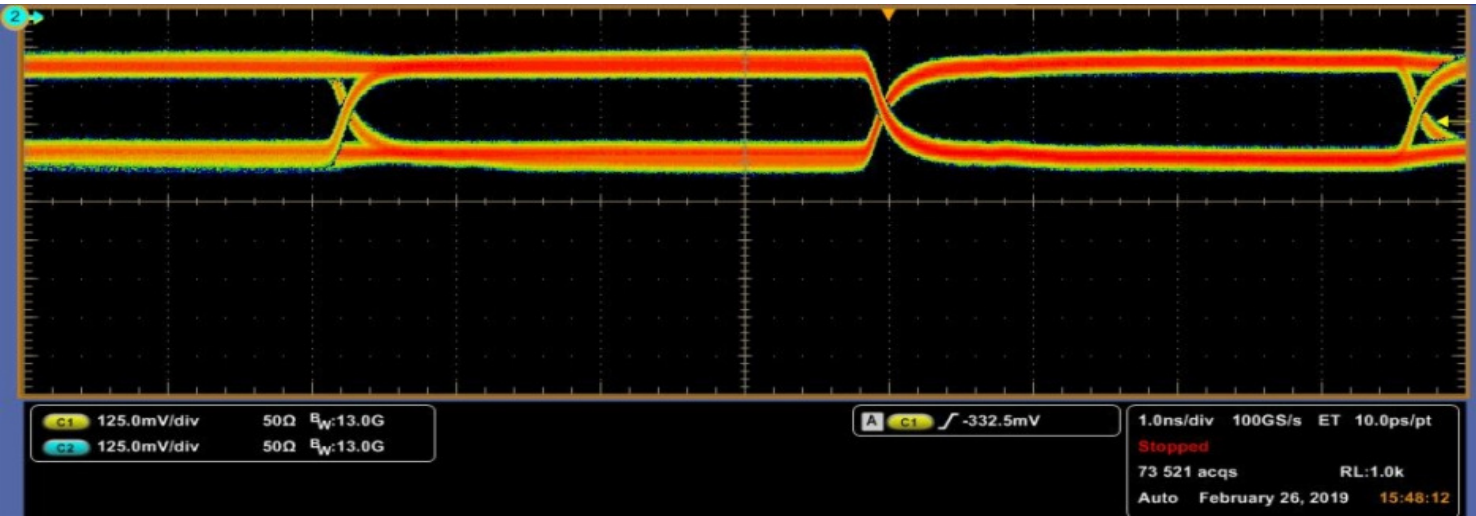


7-7 : Source Intra-Pair Skew : D0

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.0*Tbit	3.7037ns	0.15*Tbit	Pass

Waveform/Plot

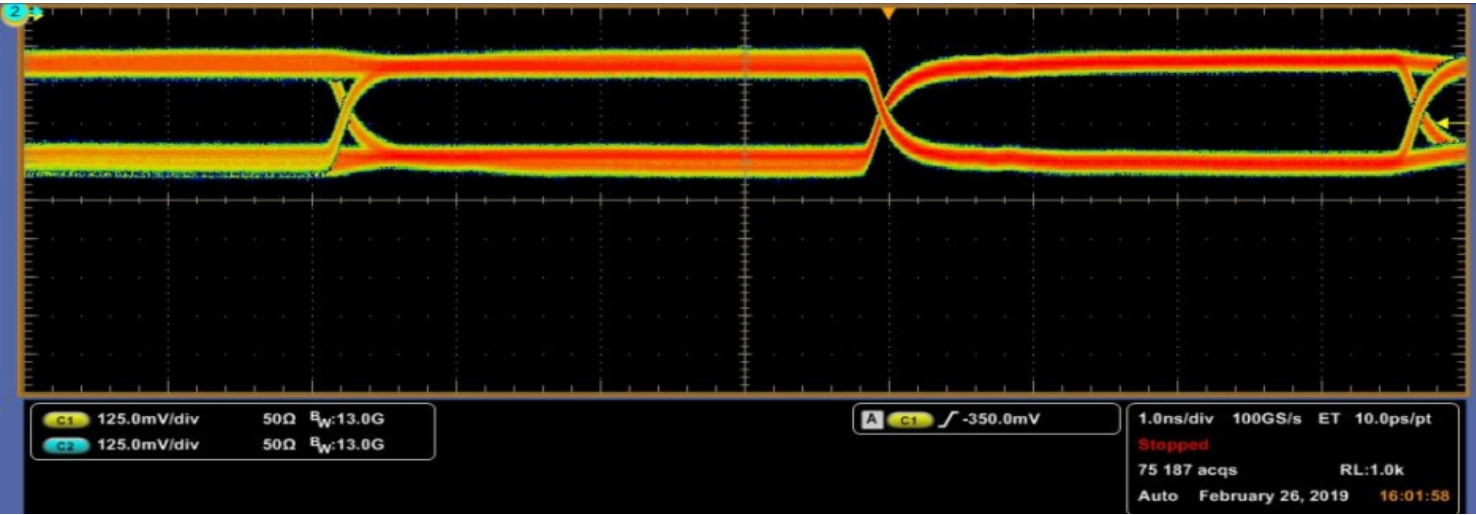


7-7 : Source Intra-Pair Skew : D1

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.0*Tbit	3.7037ns	0.15*Tbit	Pass

Waveform/Plot

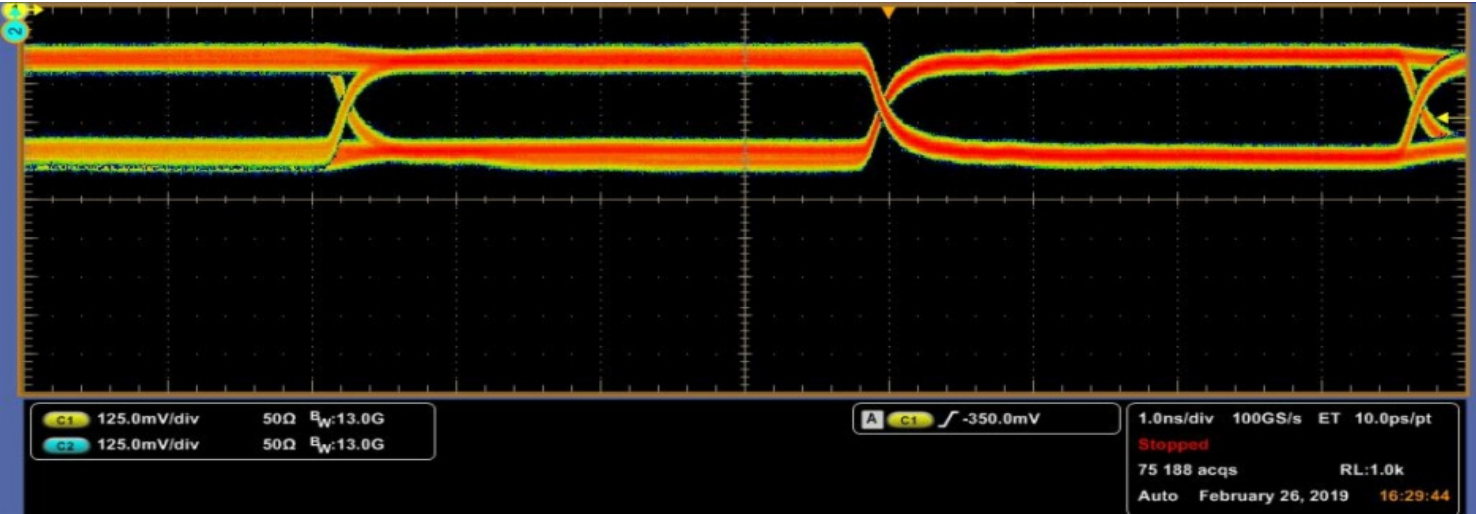


▶ 7-7 : Source Intra-Pair Skew : D2

▶ Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.003*Tbit	3.7037ns	0.15*Tbit	Pass

▶ Waveform/Plot



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