

HDMI Compliance Test Software: Measurement Report



Wed Apr 17 18:24:35 GMT 2019

Source Tests Report

► Configuration

► Setup Configuration

Oscilloscope Info MSO71604C - 10.8.7 Build 25
TDSHT3 Version 5.3.6 Build 54

► Device Configuration

Device Details HDMI Device
Clock Frequency(Mhz) 74.1761
Resolution 1080i_60Hz
Refresh Rate 60Hz

► Compliance Summary

Total Tests Supported 9
Tests Completed 21
Pass 21
Fail 0

► Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.056*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.05*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.07*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.05*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.007*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0.006*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D0 - D2	Skew < 0.2*TPixel;	0.006*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	218.74ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	229.22ps	Pass
10	7-4 : Source Fall Time	CK	75.00ps < TFALL;	219.53ps	Pass
11	7-4 : Source Fall Time	D0	75.00ps < TFALL;	223.41ps	Pass
12	7-4 : Source Rise Time	D1	75.00ps < TRISE;	229.66ps	Pass
13	7-4 : Source Fall Time	D1	75.00ps < TFALL;	226.69ps	Pass
14	7-4 : Source Rise Time	D2	75.00ps < TRISE;	247.66ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	246.74ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.74%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.85%	Pass
18	7-7 : Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.059*Tbit	Pass
19	7-7 : Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.056*Tbit	Pass
20	7-7 : Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.053*Tbit	Pass
21	7-7 : Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.047*Tbit	Pass

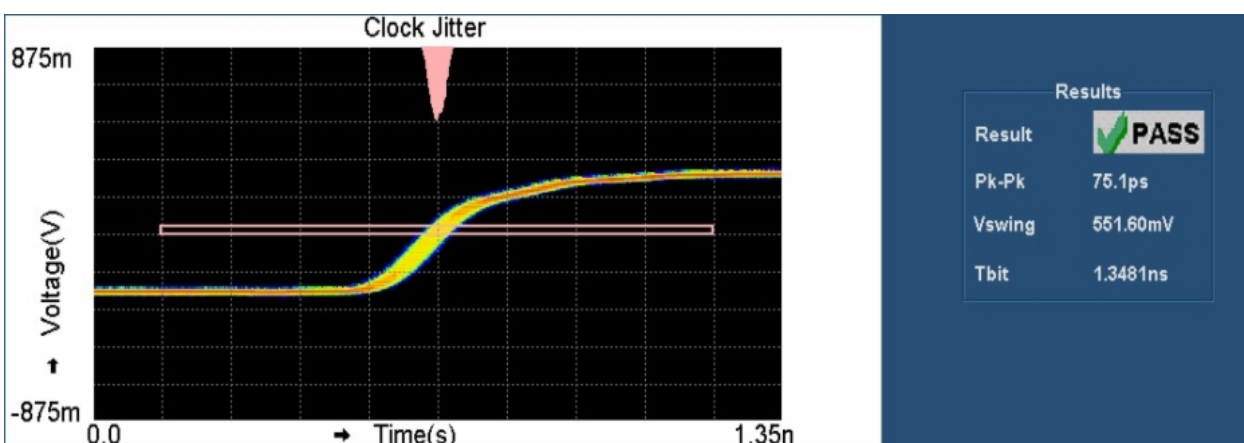
► Detailed Results

► 7-9 : Source Clock Jitter : CK

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Result
Clock Jitter < 0.25*Tbit;	0.056*Tbit	1.3481ns	551.60mV	0.19*Tbit	50.000M	Pass

► Waveform/Plot

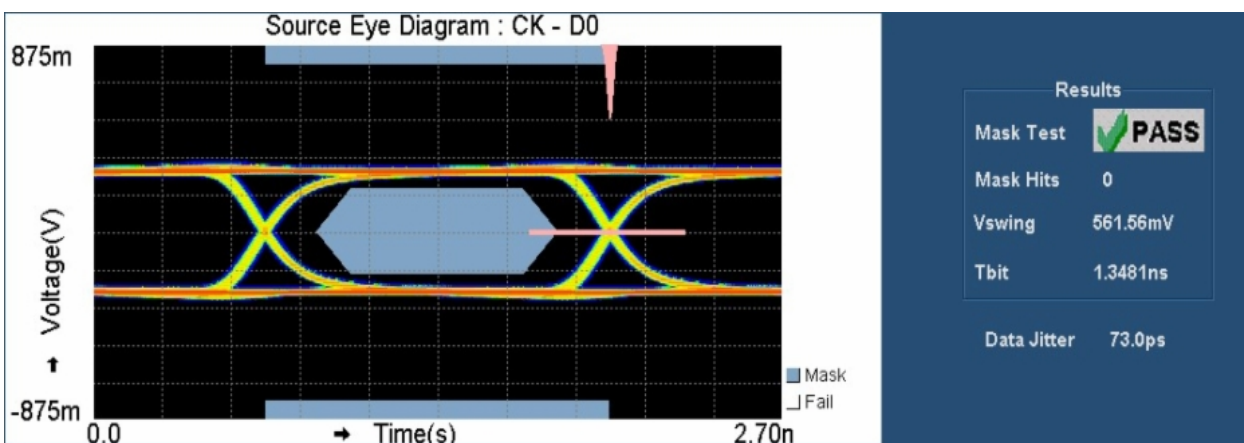


► 7-10 : Source Eye Diagram : CK - D0

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.05*Tbit	1.3481ns	561.56mV	245.8m*Tbit	50.000M	0	Pass

► Waveform/Plot

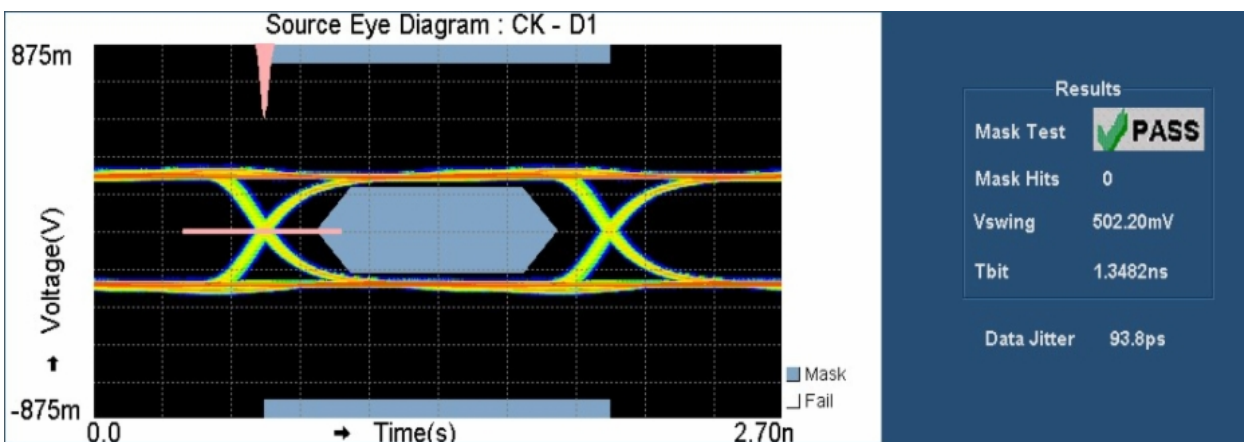


► 7-10 : Source Eye Diagram : CK - D1

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.07*Tbit	1.3482ns	502.20mV	230.4m*Tbit	50.000M	0	Pass

► Waveform/Plot

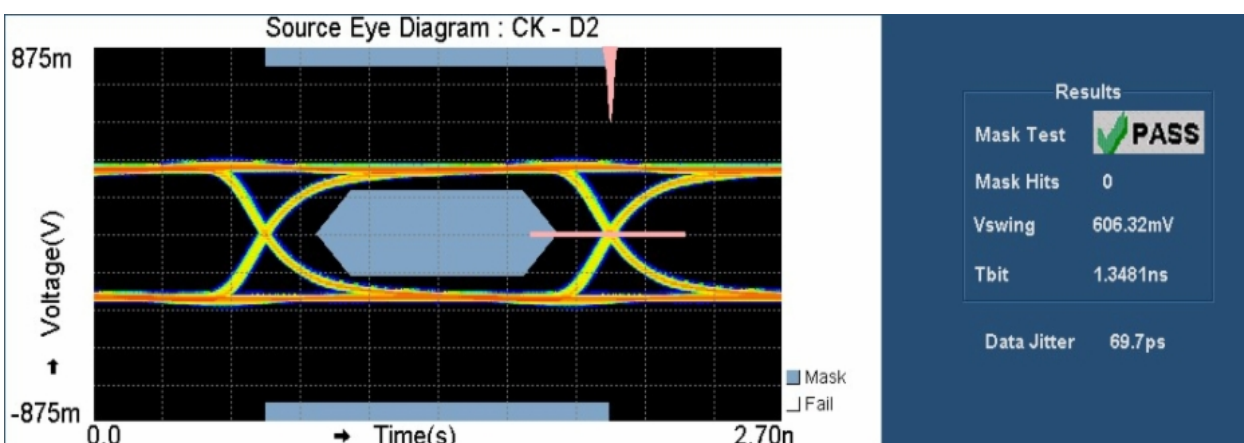


► 7-10 : Source Eye Diagram : CK - D2

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.05*Tbit	1.3481ns	606.32mV	248.3m*Tbit	50.000M	0	Pass

► Waveform/Plot



► 7-6 : Source Inter-Pair Skew : D0 - D1

► Results

Spec Range	Meas Value	Tbit	Vs(D0 - D1)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.007*TPixel	1.3481ns	= 564.00mV, Vs = 510.30mV	98.586p	103.06p	100.13p	Pass

► 7-6 : Source Inter-Pair Skew : D1 - D2

► Results

Spec Range	Meas Value	Tbit	Vs(D1 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.006*TPixel	1.3481ns	= 502.74mV, Vs = 610.56mV	78.077p	84.833p	81.769p	Pass

► 7-6 : Source Inter-Pair Skew : D0 - D2

► Results

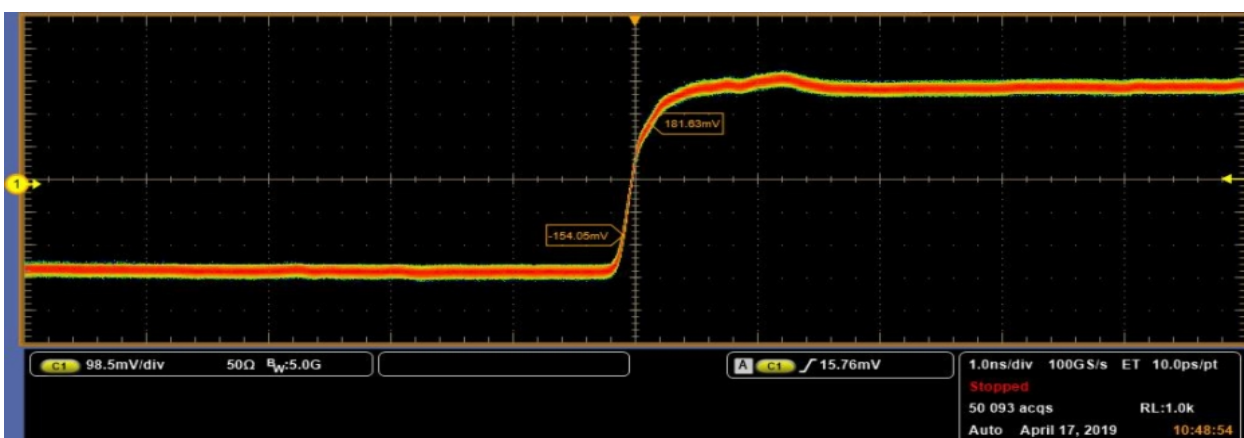
Spec Range	Meas Value	Tbit	Vs(D0 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.006*TPixel	1.3481ns	= 564.00mV, Vs = 612.04mV	79.722p	84.530p	82.305p	Pass

► 7-4 : Source Rise Time : CK

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	218.74ps	1.3481ns	559.48mV	143.7ps	Pass

► Waveform/Plot

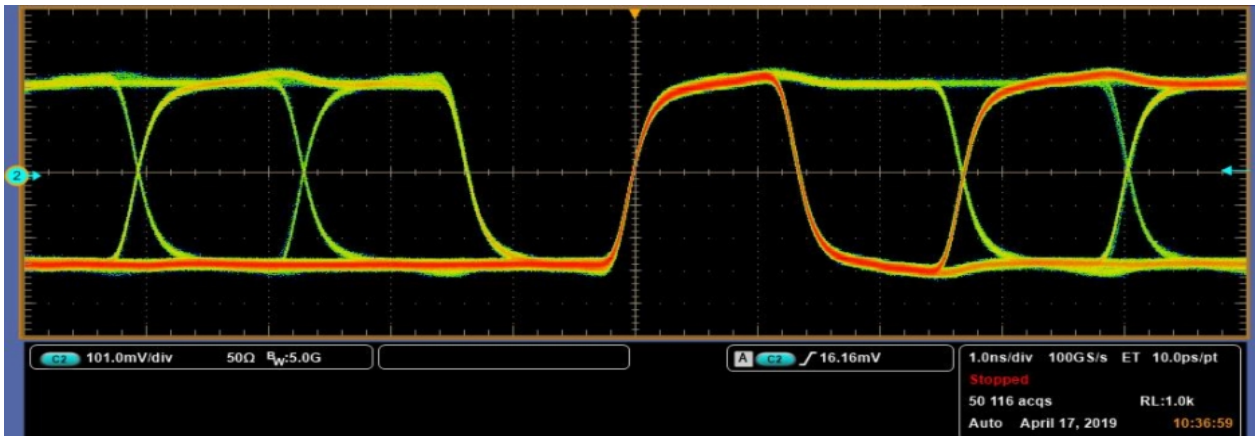


► 7-4 : Source Rise Time : D0

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	229.22ps	1.3481ns	561.56mV	154.2ps	Pass

► Waveform/Plot

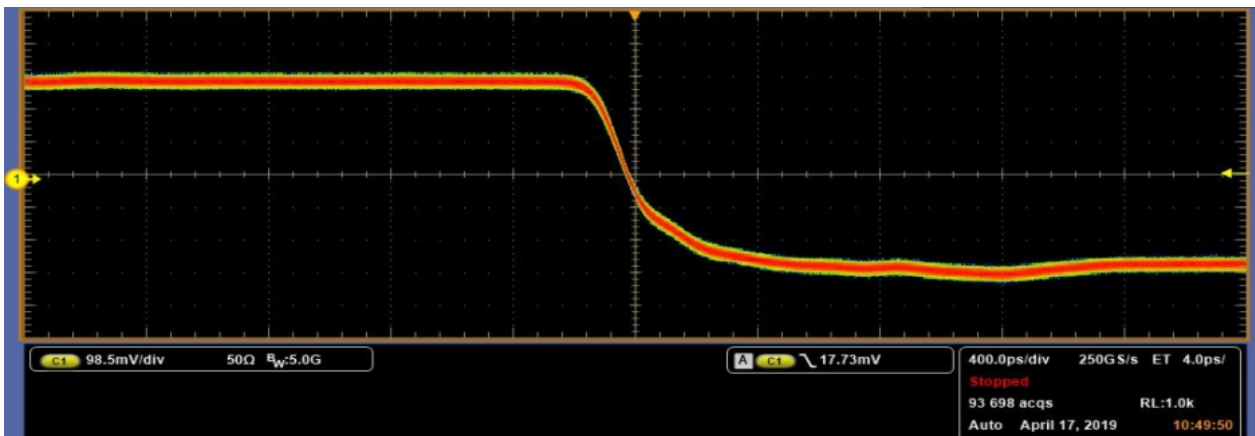


► 7-4 : Source Fall Time : CK

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	219.53ps	1.3481ns	559.48mV	144.5ps	Pass

► Waveform/Plot

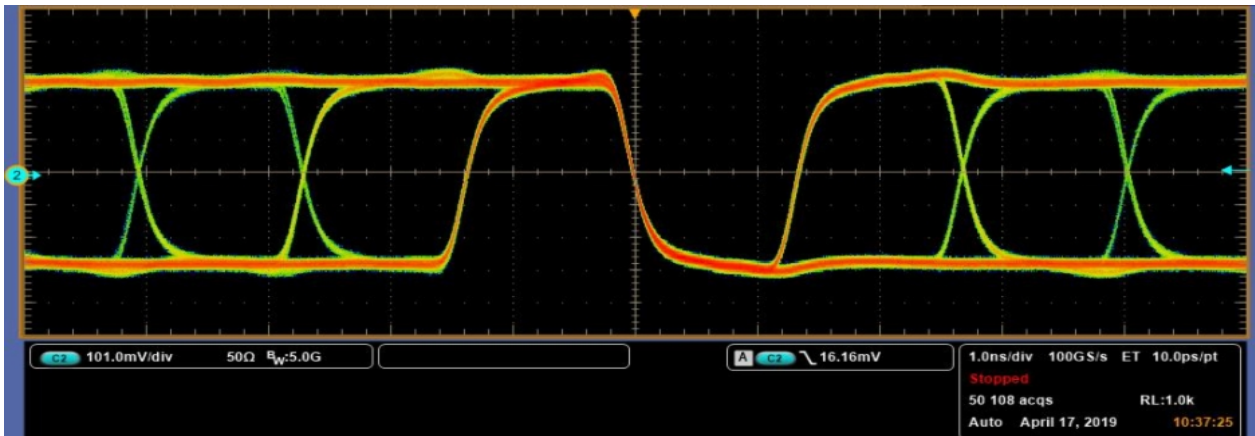


► 7-4 : Source Fall Time : D0

► Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	223.41ps	1.3481ns	561.56mV	148.4ps	Pass

► Waveform/Plot

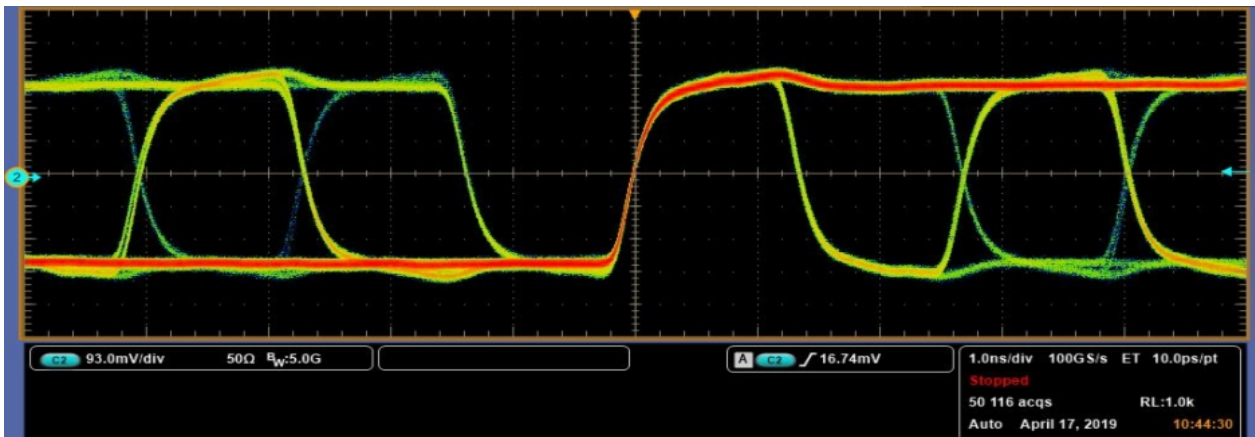


7-4 : Source Rise Time : D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	229.66ps	1.3482ns	502.20mV	154.7ps	Pass

Waveform/Plot

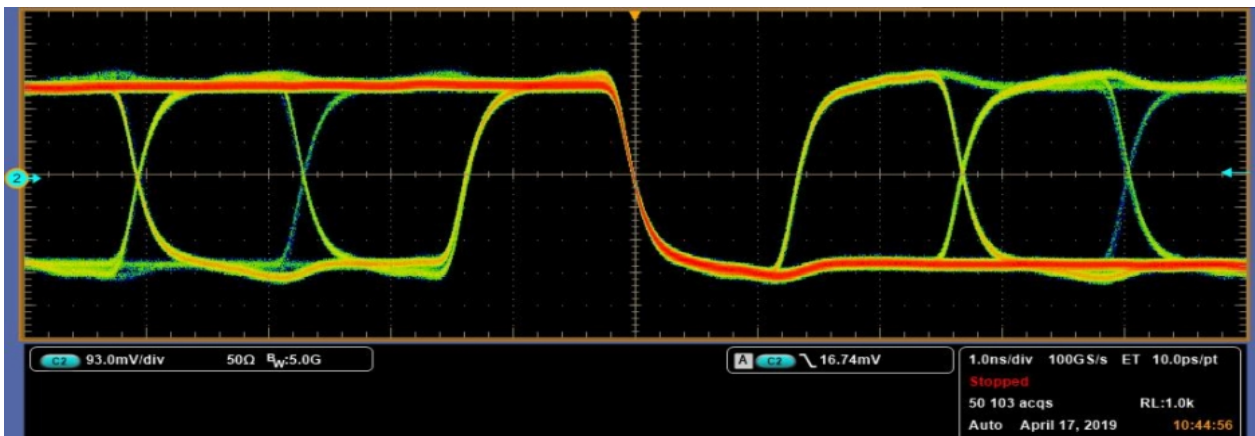


7-4 : Source Fall Time : D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	226.69ps	1.3482ns	502.20mV	151.7ps	Pass

Waveform/Plot

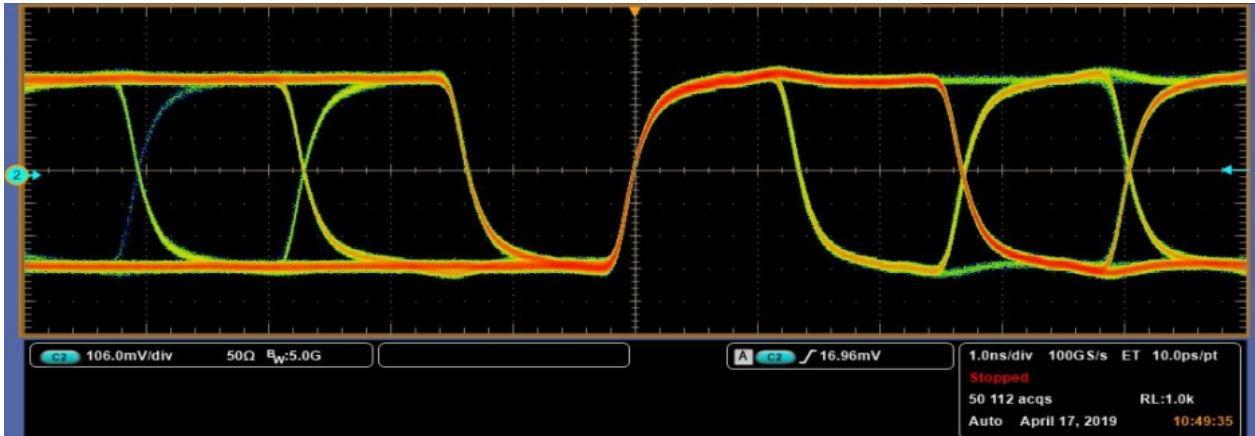


7-4 : Source Rise Time : D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	247.66ps	1.3481ns	602.08mV	172.7ps	Pass

Waveform/Plot

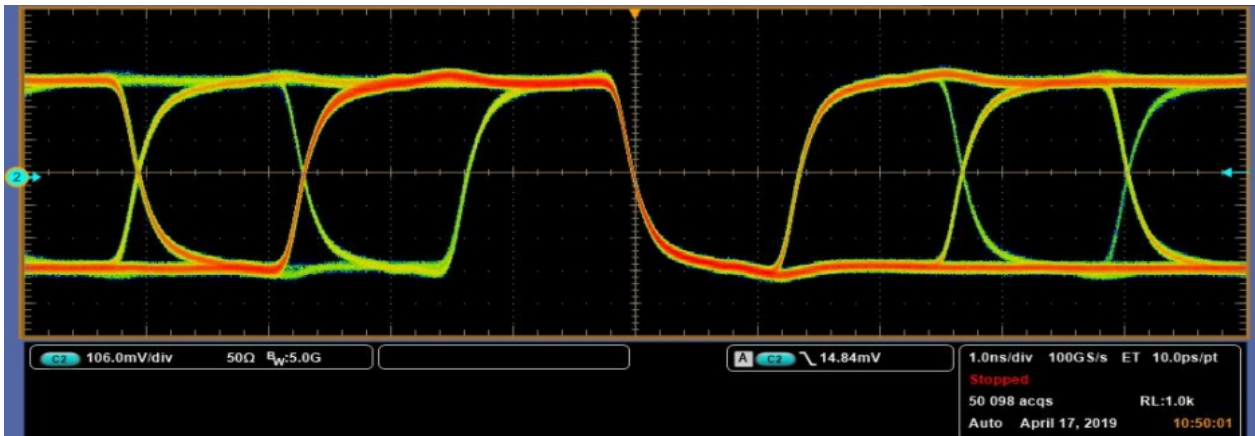


7-4 : Source Fall Time : D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	246.74ps	1.3481ns	602.08mV	171.7ps	Pass

Waveform/Plot

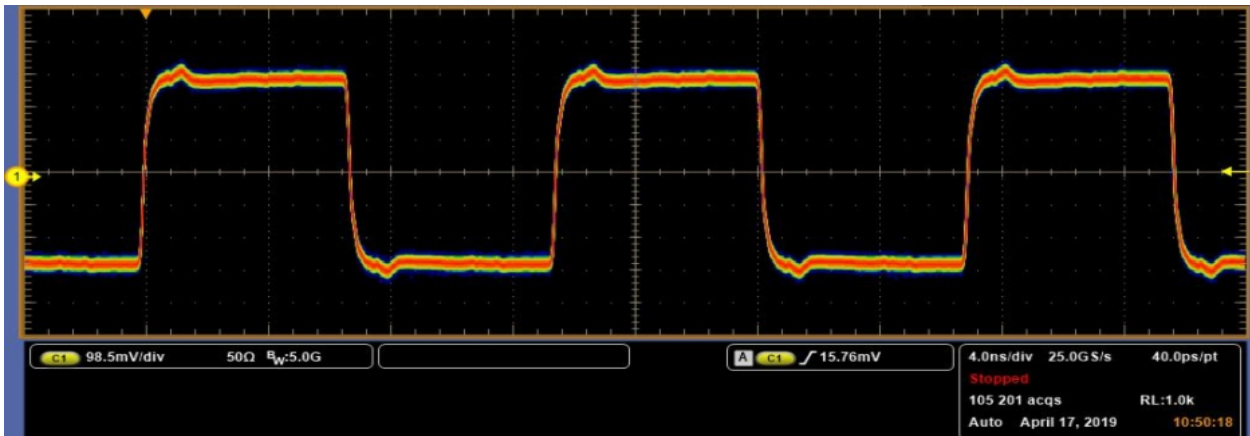


7-8 : Max Duty Cycle : CK

Results

Spec Range	Meas Value	Tbit	Margin	Result
Max Duty Cycle < 60.0%;	50.74%	1.3481ns	9.26%	Pass

Waveform/Plot

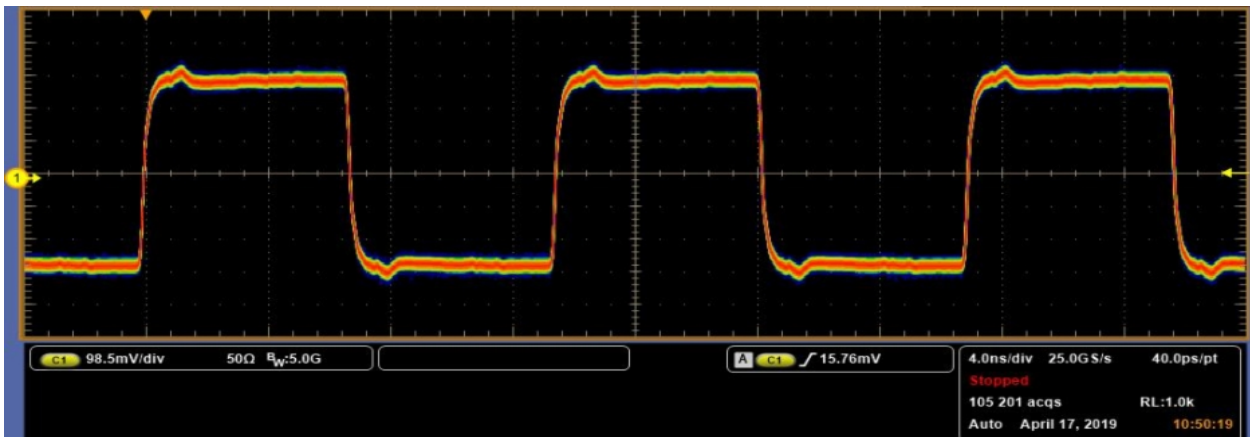


7-8 : Min Duty Cycle : CK

Results

Spec Range	Meas Value	Tbit	Margin	Result
40.0% < Min Duty Cycle;	49.85%	1.3481ns	9.85%	Pass

Waveform/Plot

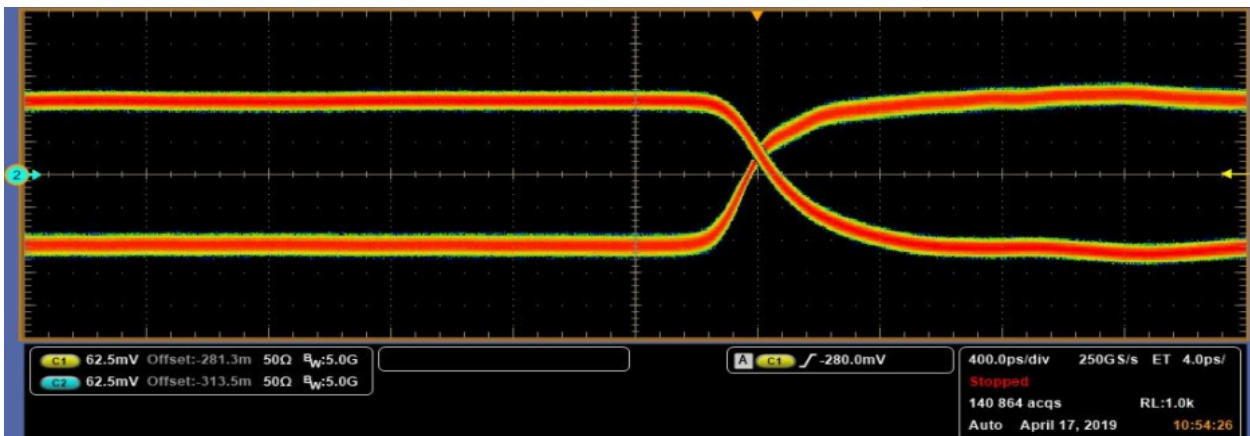


7-7 : Source Intra-Pair Skew : CK

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.059*Tbit	1.3481ns	0.09*Tbit	Pass

Waveform/Plot

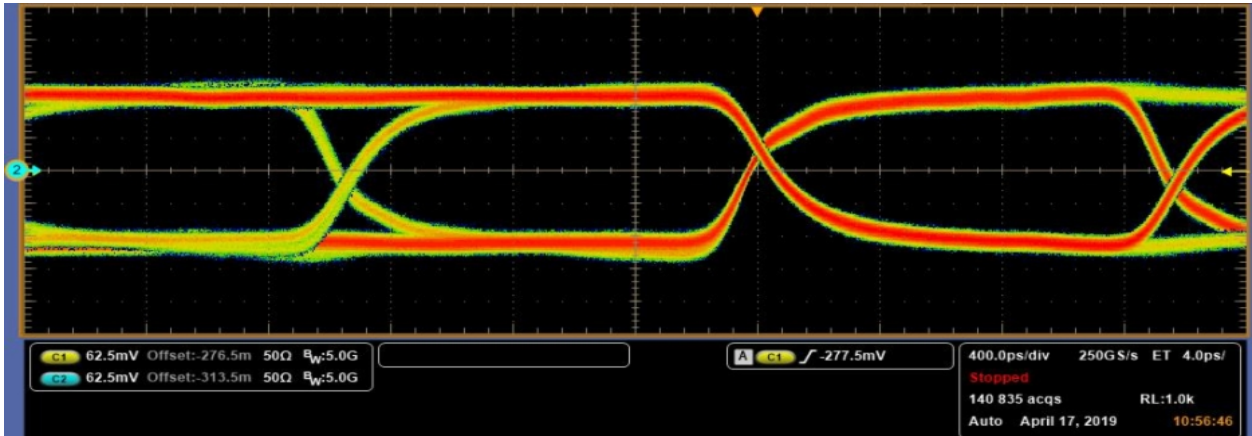


► 7-7 : Source Intra-Pair Skew : D0

► Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.056*Tbit	1.3481ns	0.09*Tbit	Pass

► Waveform/Plot

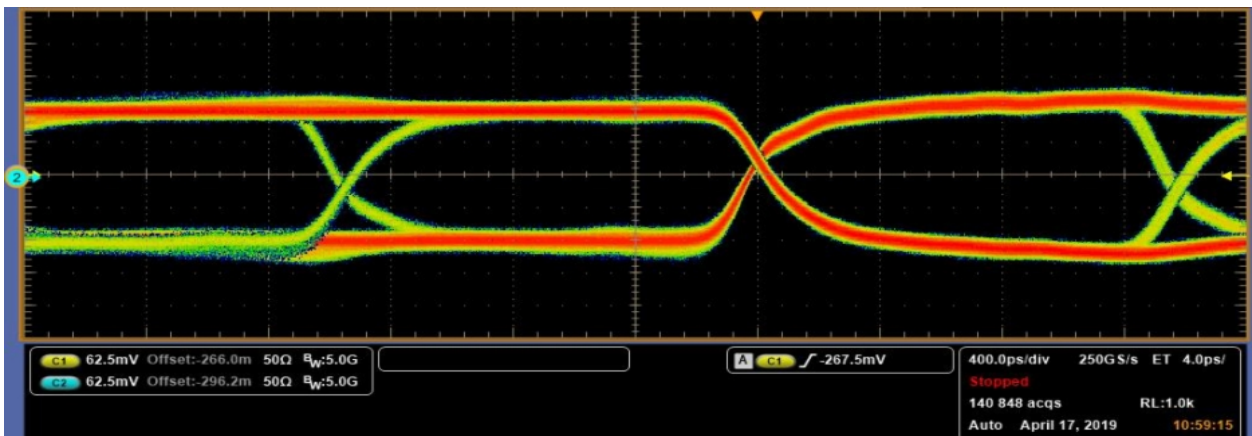


► 7-7 : Source Intra-Pair Skew : D1

► Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.053*Tbit	1.3481ns	0.1*Tbit	Pass

► Waveform/Plot

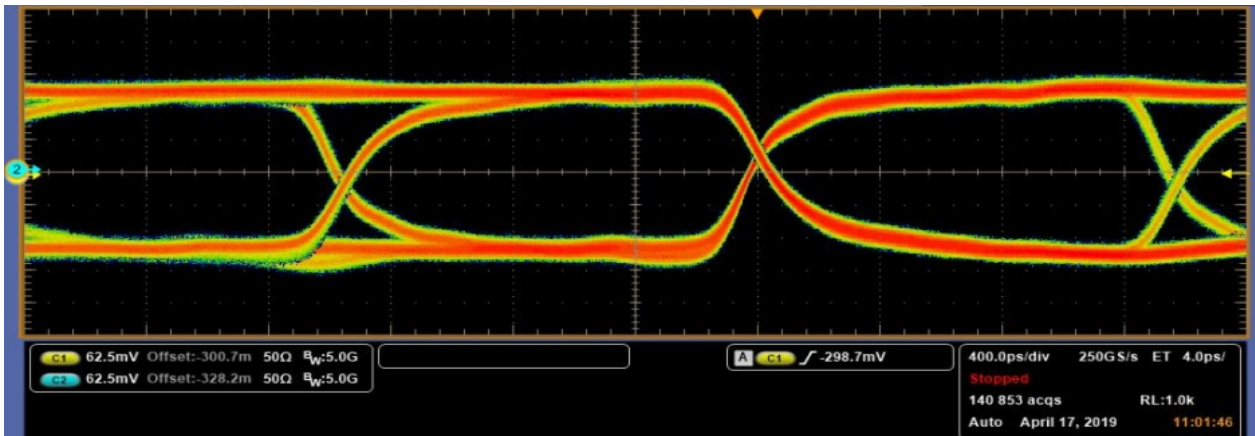


► 7-7 : Source Intra-Pair Skew : D2

► Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.047*Tbit	1.3481ns	0.1*Tbit	Pass

► Waveform/Plot



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