

Signal Integrity Simulation Report

Project: K18X001T00_DDR4-2400_Post Simulation
Date: 2020/08/17

	Author
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Simulation Conditions

- Simulation board file: K18X001T00_005.brd
- Simulation model:

Component	IBIS / Spice Model Name	Version / Provider
Controller	BG5CT_IBIS_Rev1r2_DDR4.ibs	Marvell
DRAM	h5an4g_xn_bjr-xi.ibs	Hynix
	h5an8g_xn_cjr.ibs	

- Pre-requisite:

Concerned factor	Not concerned
XTALK	Trace temperature
IC model corners (Fast/Typ/Slow)	Manufacture variation
TX drive strength & RX ODT	
Power SSN to SI effects	

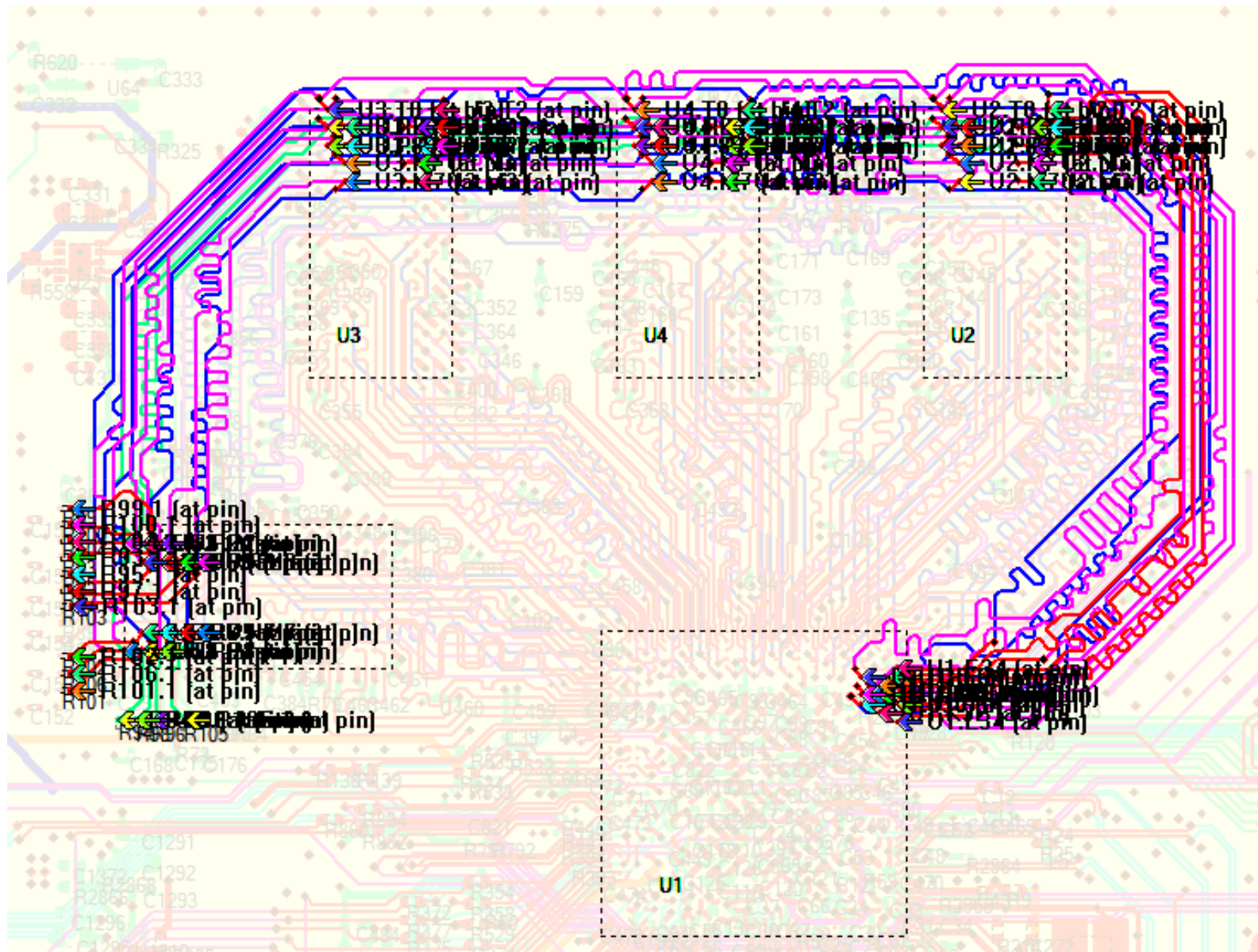
Note:

1. The XTALK have include nets with coupled voltage greater than 120mV, and considered in waveform simulation with sensitive aggressors.
2. The simulation are from die-to-die (include package) results.
3. CPU temperature Range @ 50C typ, 125C slow, 0C fast
DRAM temperature Range @ 25C typ, 95C slow, -40C fast

- Stackup:

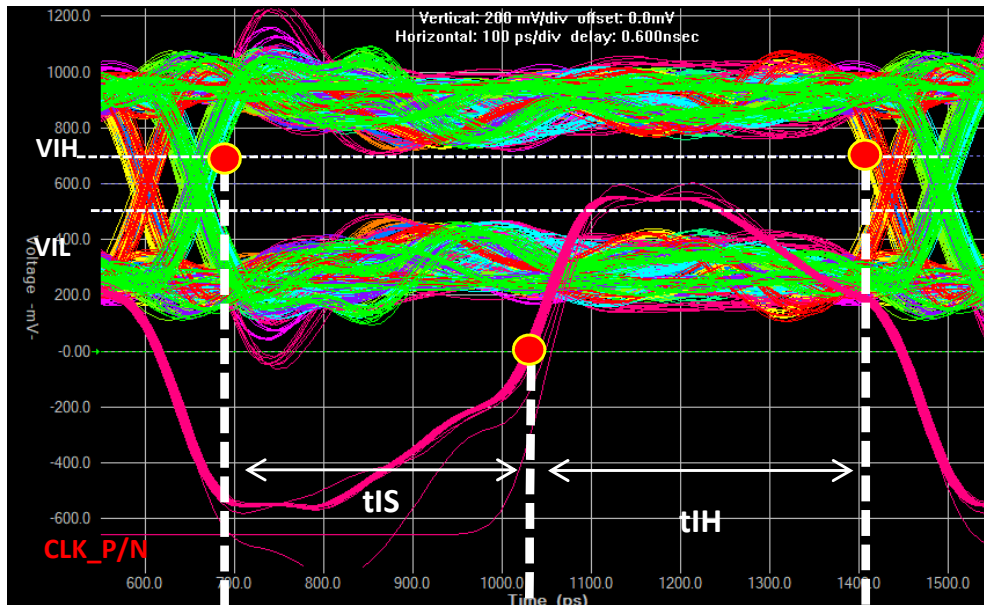
Layer Name	Type	Usage	Thickness mils	Er	Test Width mils	Z0 ohm
DIE_001	Dielectric	Solder Mask	0.4	4		
TOP	Metal	Signal	1.8	<Auto>	5	50.1
DIE_003	Dielectric	Substrate	3.2	3.91		
MID1_L2_	Metal	Plane	1.2	<Auto>	16	58.6
DIE_005	Dielectric	Substrate	4	4		
MID2_L3_	Metal	Signal	1.2	<Auto>	5	49.7
DIE_007	Dielectric	Substrate	15.95	4.17		
MID3_L4_	Metal	Signal	1.2	<Auto>	16	56.3
DIE_009	Dielectric	Substrate	4	4.36		
MID4_L5_	Metal	Signal	1.2	<Auto>	15	57.9
DIE_011	Dielectric	Substrate	15.95	4.17		
MID5_L6_	Metal	Signal	1.2	<Auto>	5	49.7
DIE_013	Dielectric	Substrate	4	4		
MID6_L7_	Metal	Plane	1.2	<Auto>	16	58.6
DIE_015	Dielectric	Substrate	3.2	3.91		
BOTTOM	Metal	Signal	1.8	<Auto>	5	50.1
DIE_017	Dielectric	Solder Mask	0.4	4		

ADD/CMD Topology

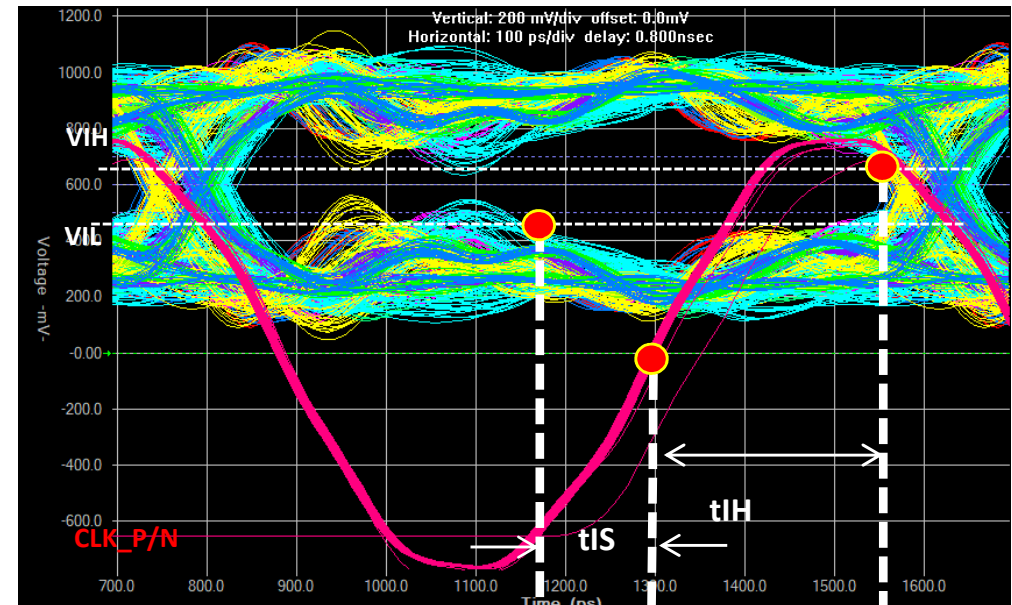


ADD/CMD Simulation Waveform (typ)

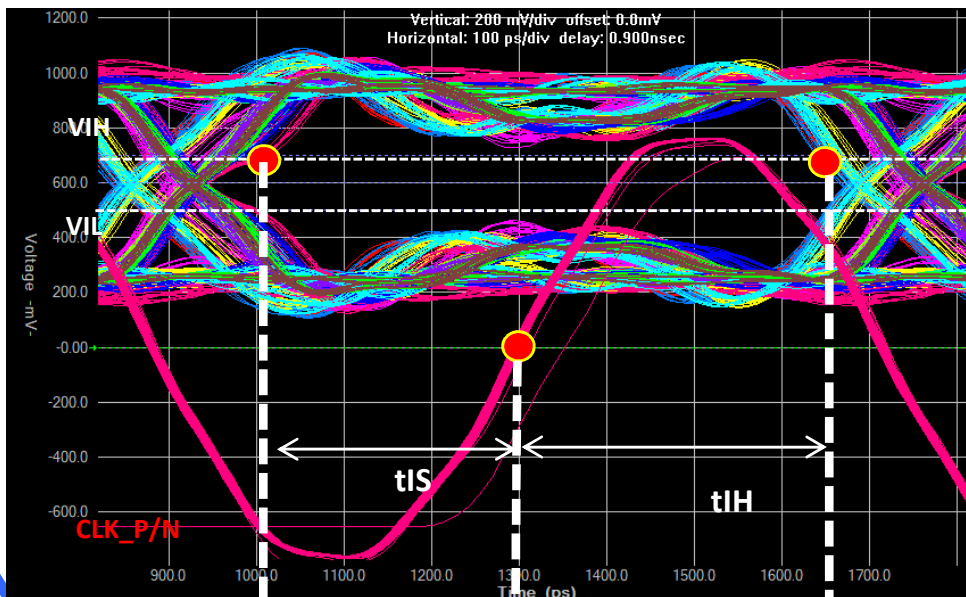
1st DDR U2



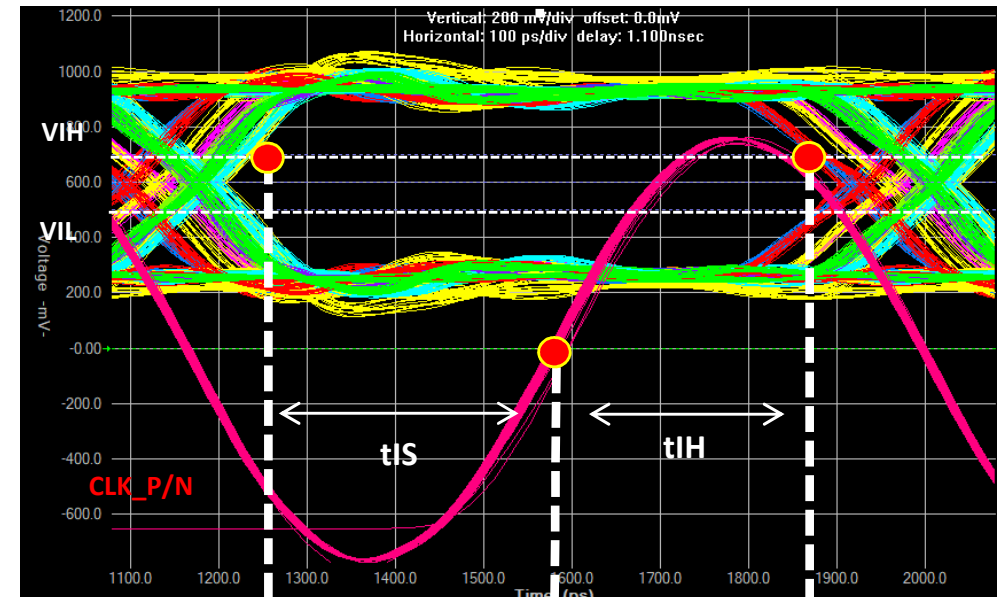
2nd DDR U4



3rd DDR U3

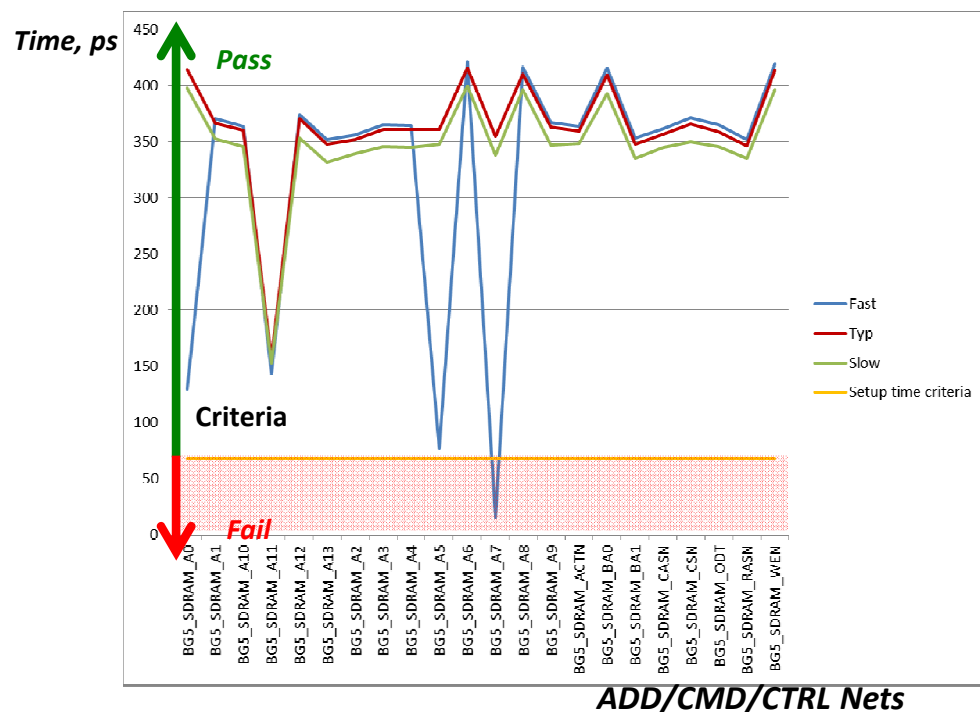


4th DDR U5

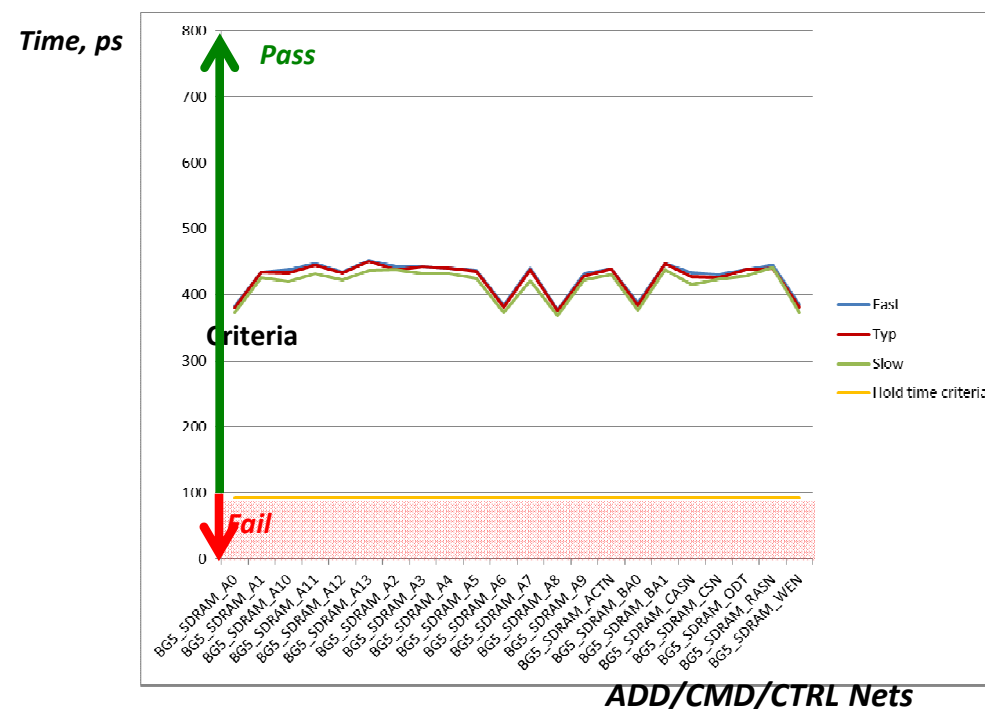


CK vs. ADD/CMD/CTRL Timing Budget @U2

Setup time budget



Hold time budget

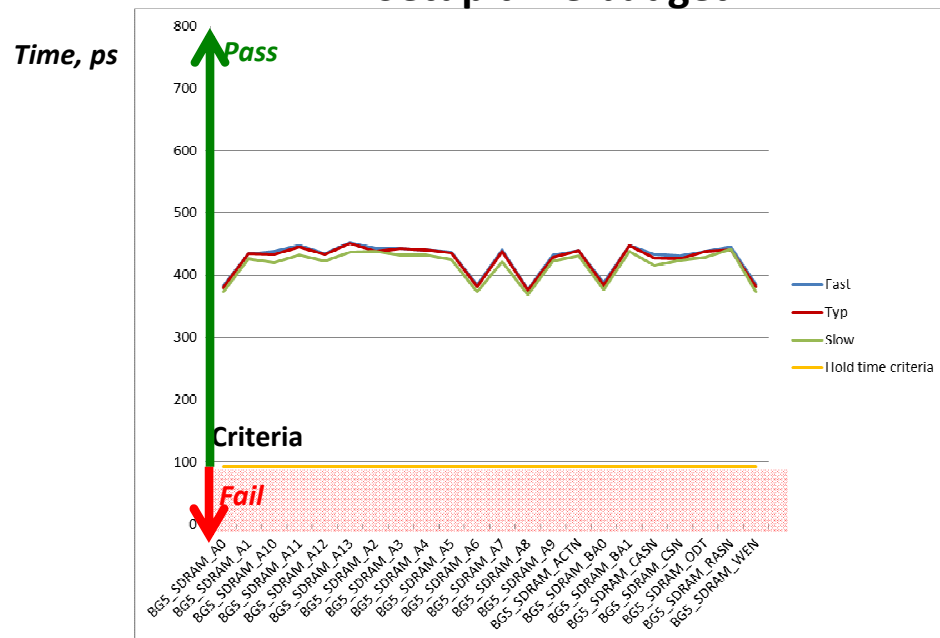


Note:

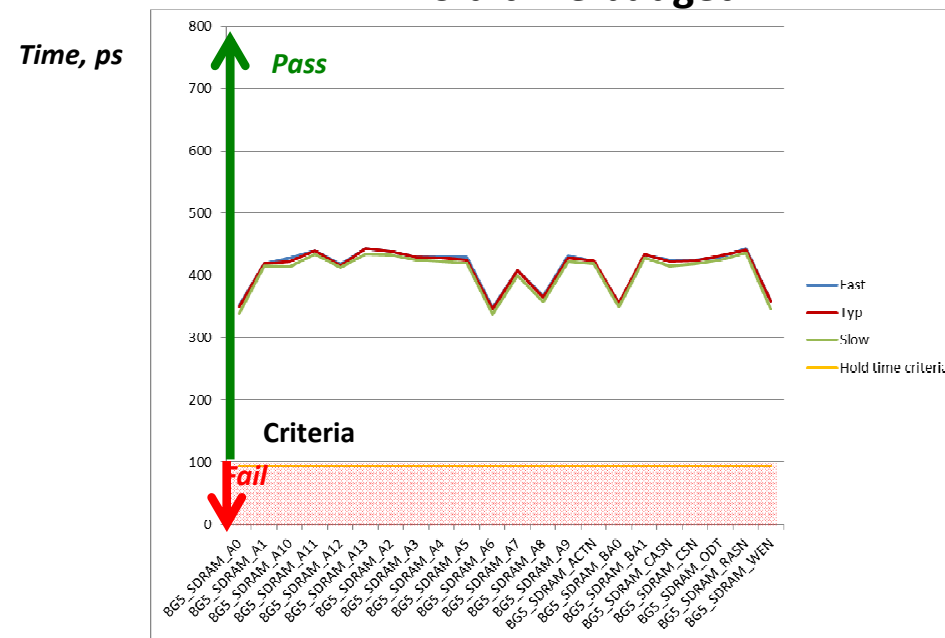
1. The setup/ hold time criteria are considered the $t_{DS,H(base)}$, $d(t_{DS,H})$ and initial delay δ .
2. The setup exist larger reflection that lead the less setup time margin especially in fast corner.
3. The simulation include different corners result.

CK vs. ADD/CMD/CTRL Timing Budget @U3

Setup time budget



Hold time budget

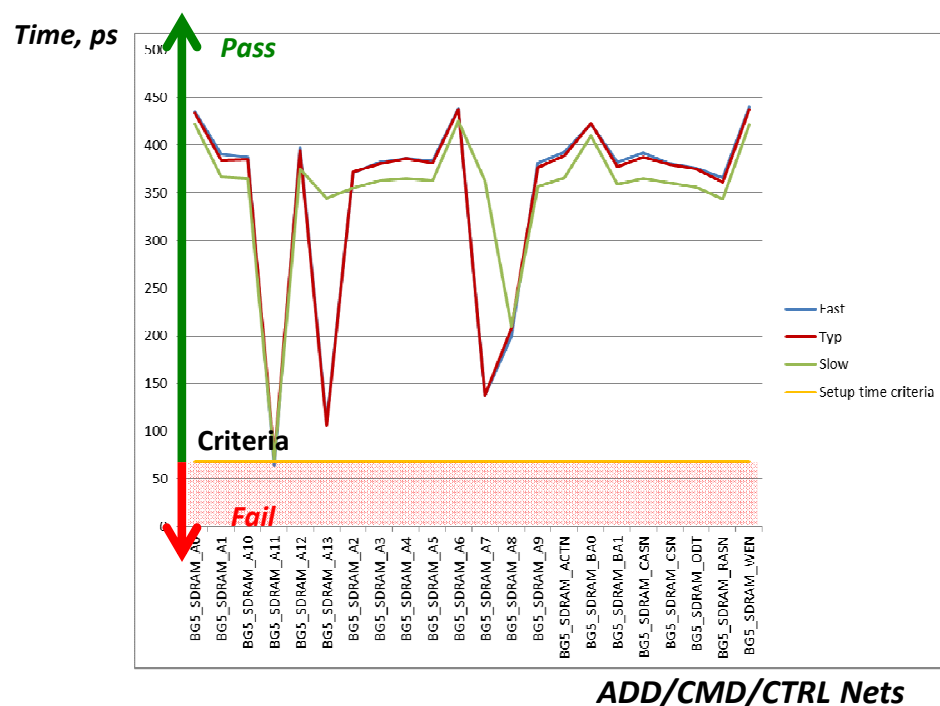


Note:

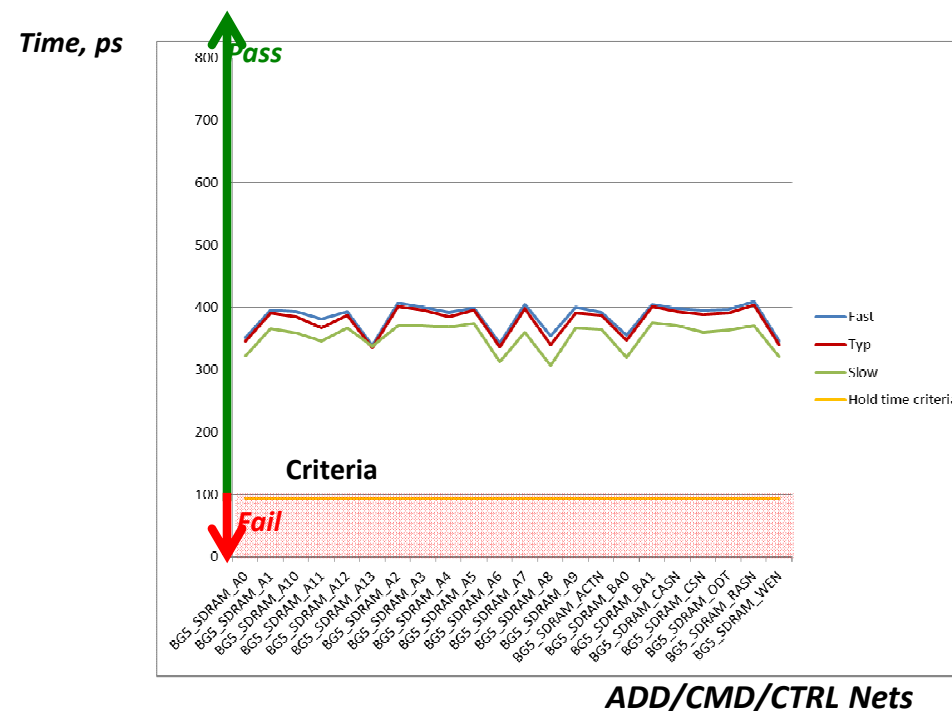
1. The setup/ hold time criteria are considered the $t_{DS,H(base)}$, $d(t_{DS,H})$ and initial delay δ .
2. Both setup/hold time margin should be within specification limit to have enough margin in each nets for pass condition.
3. The simulation include different corners result.

CK vs. ADD/CMD/CTRL Timing Budget @U4

Setup time budget



Hold time budget

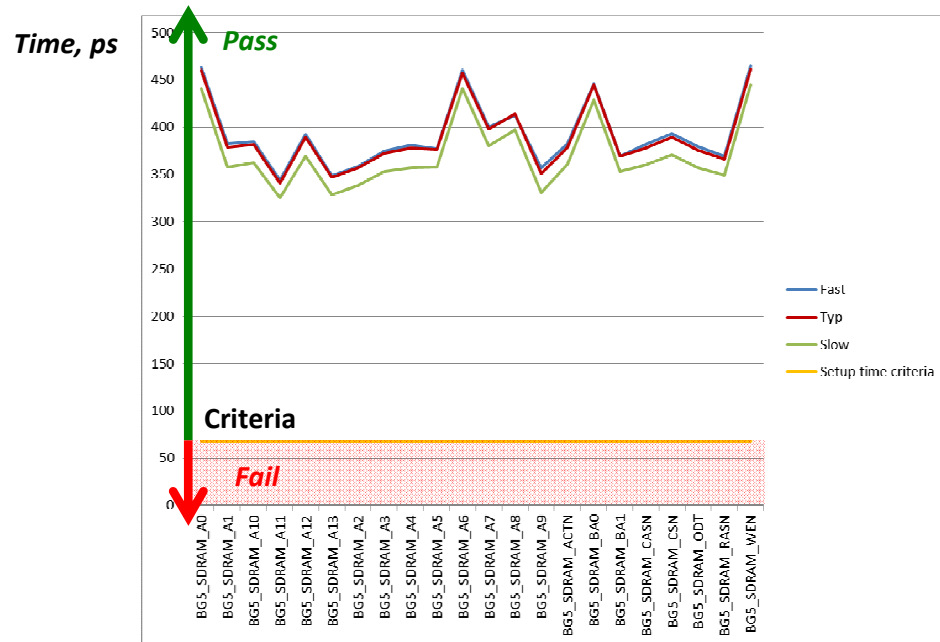


Note:

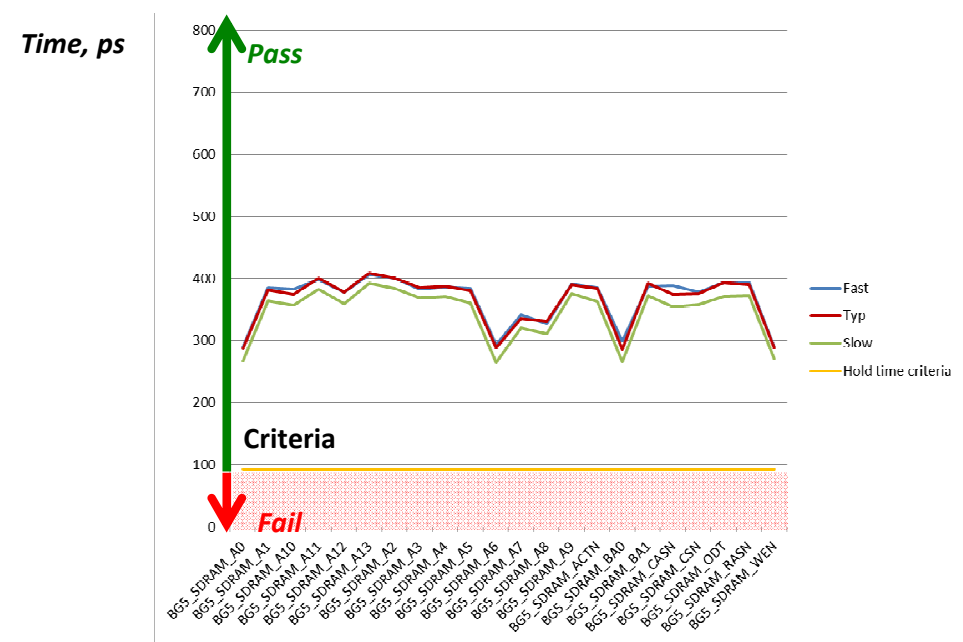
1. The setup/ hold time criteria are considered the $t_{DS,H(base)}$, $d(t_{DS,H})$ and initial delay δ .
2. The setup exist larger reflection that lead the less setup time margin especially in fast corner.
3. The simulation include different corners result.

CK vs. ADD/CMD/CTRL Timing Budget @U5

Setup time budget



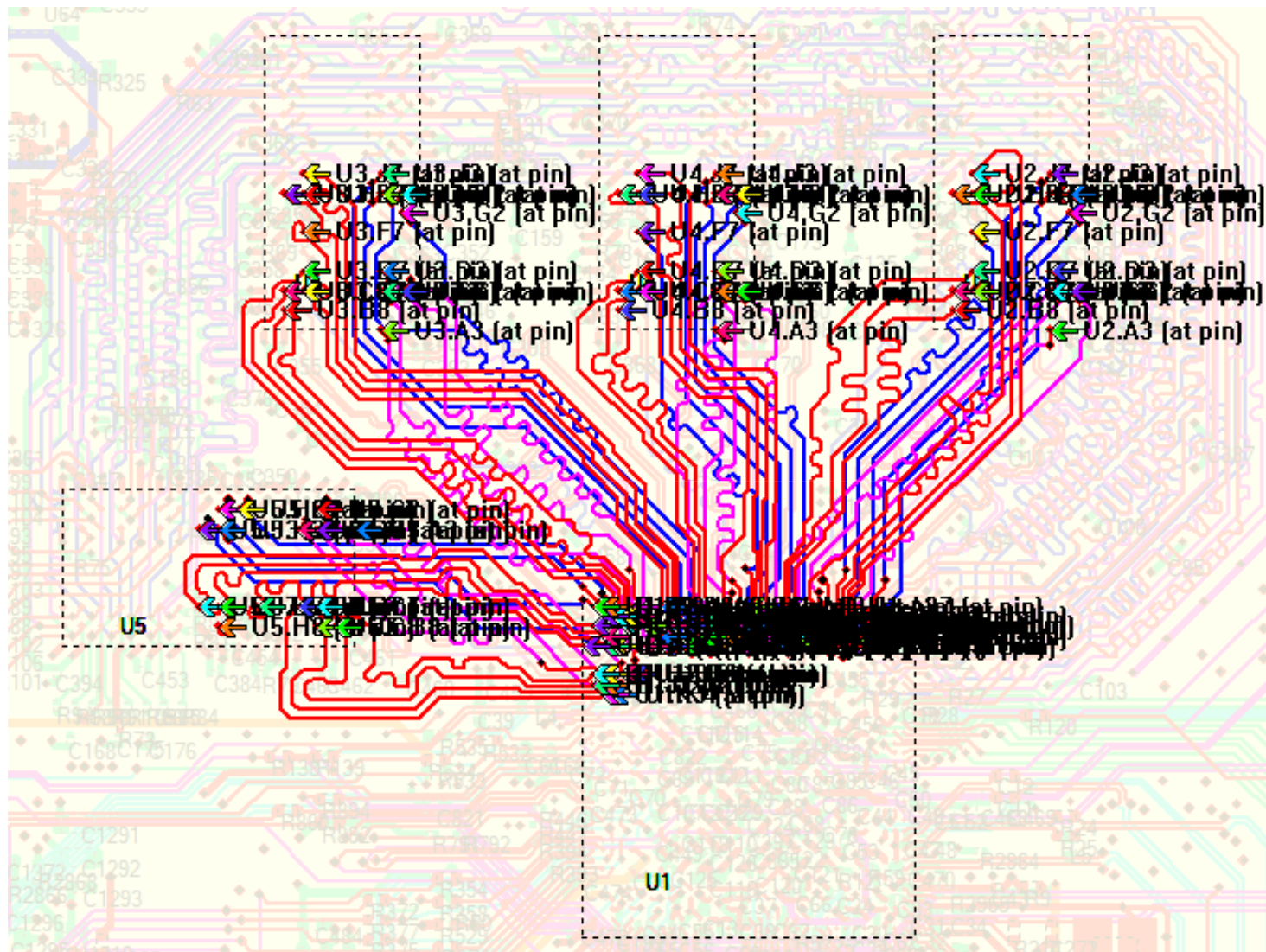
Hold time budget



Note:

1. The setup/ hold time criteria are considered the $t_{DS,H(base)}$, $d(t_{DS,H})$ and initial delay δ .
2. Both setup/hold time margin should be within specification limit to have enough margin in each nets for pass condition.
3. The simulation include different corners result.

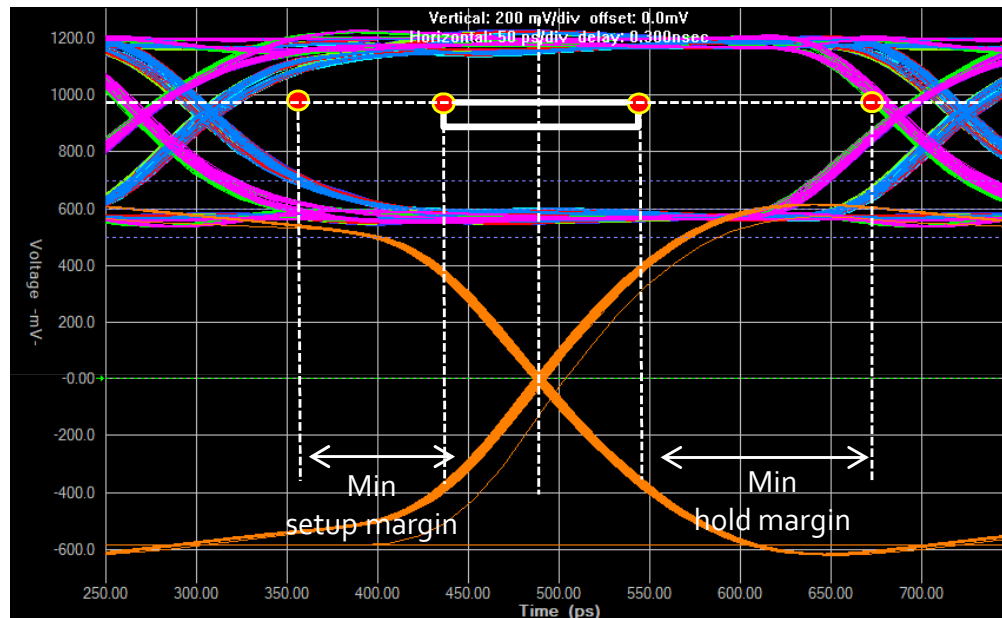
DQ Topology



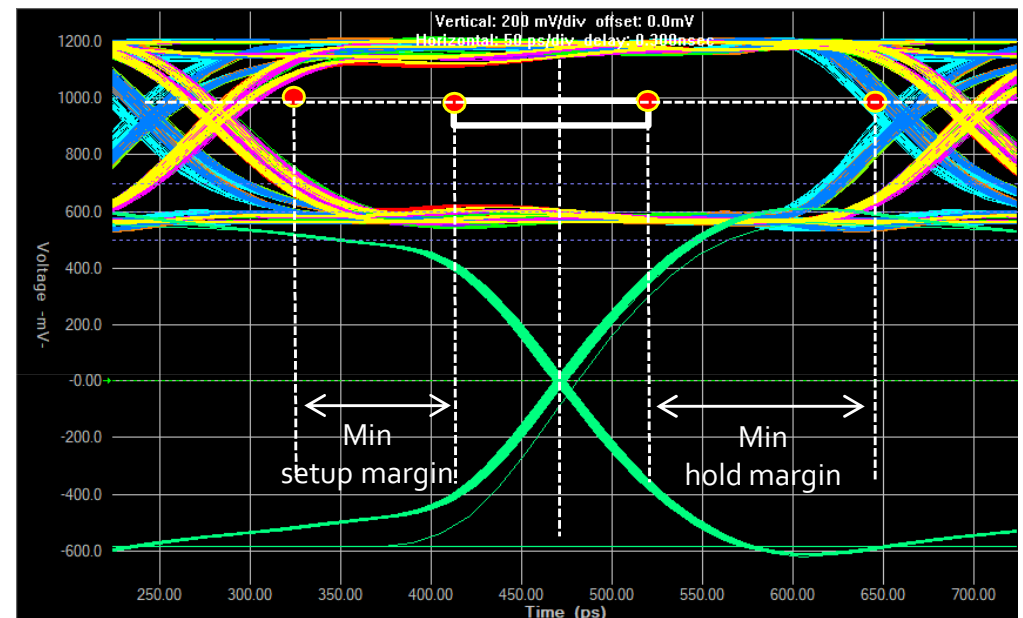
Data Write Simulation Waveform(typ)

CPU Driver → DRAM Received @die:

DQS0 vs. DQ[0:7]



DQS1 vs. DQ[8:15]

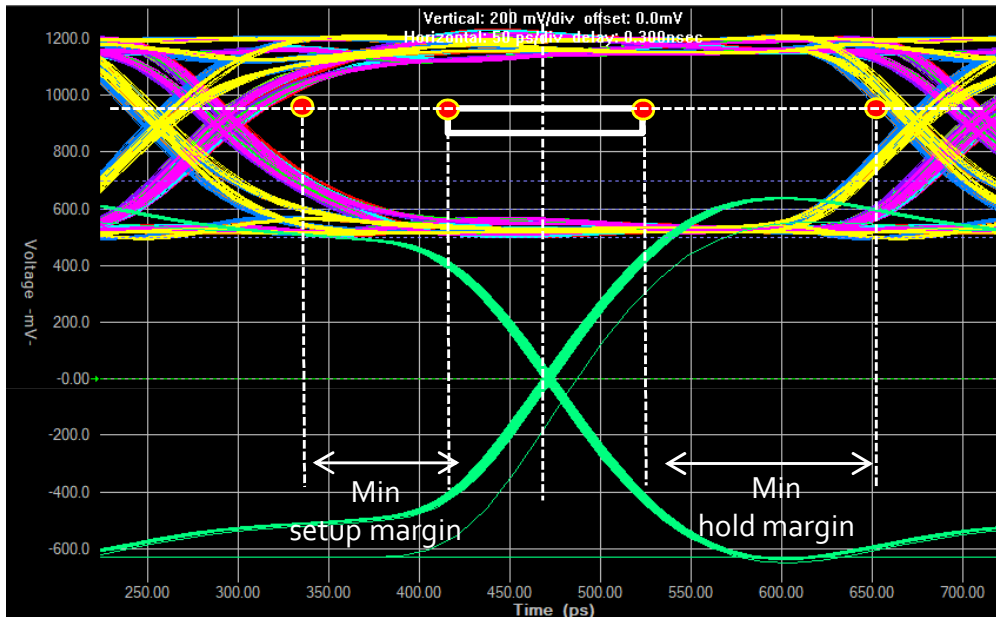


Note:

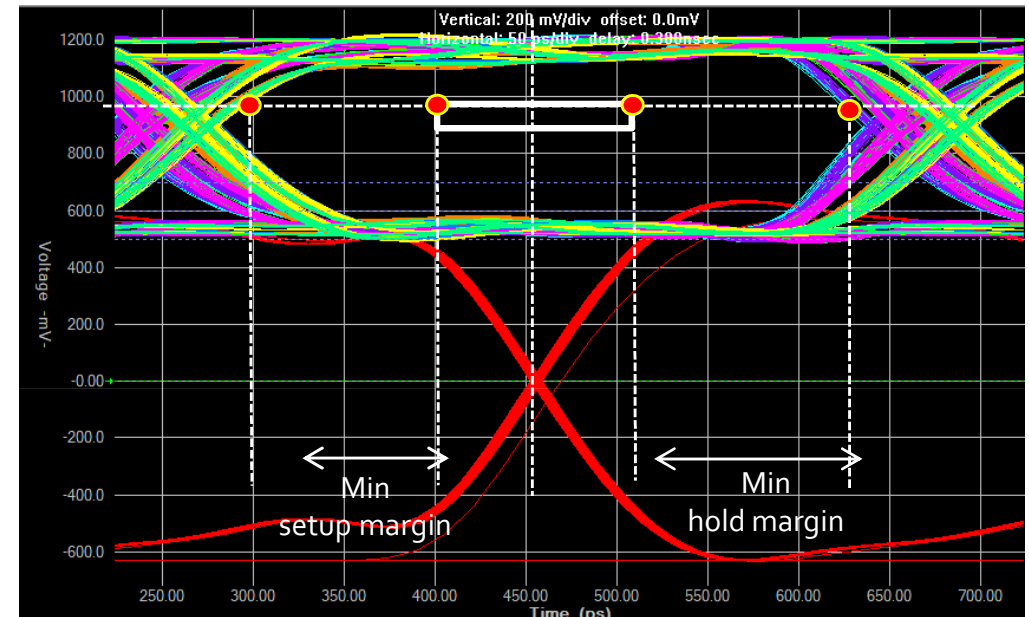
The purpose of this simulation is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

Data Write Simulation Waveform(typ) CPU Driver → DRAM Received @die:

DQS2 vs. DQ[16:23]



DQS3 vs. DQ[24:31]



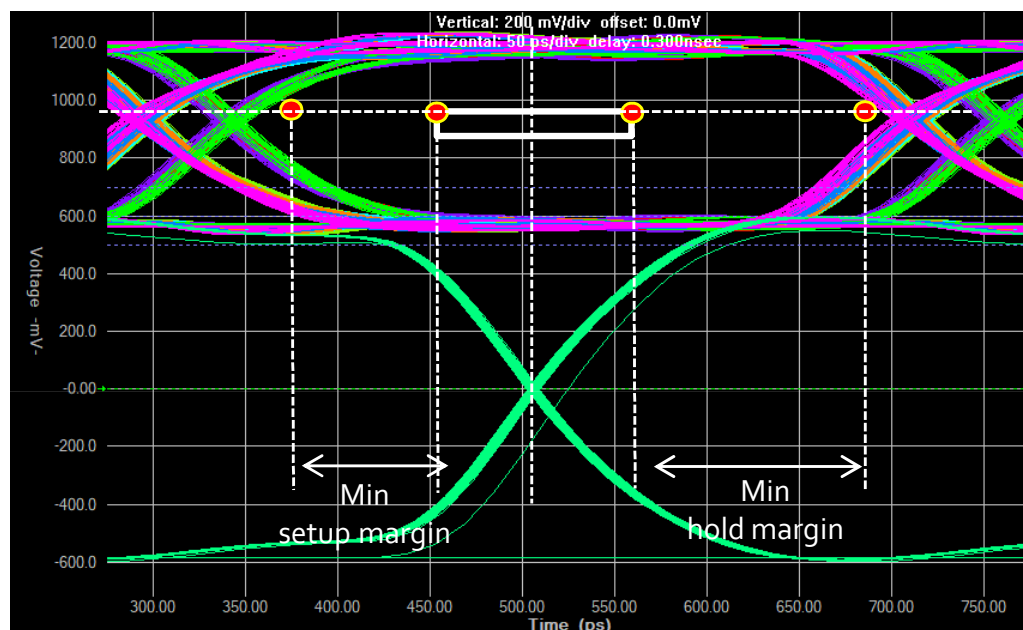
Note:

The purpose of this simulation is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

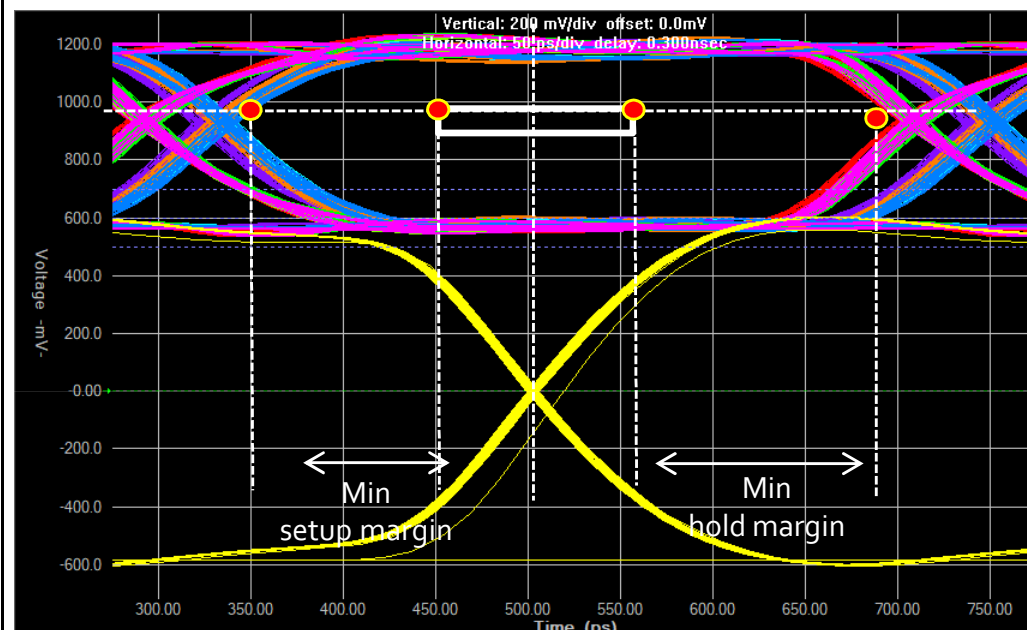
Data Write Simulation Waveform(typ)

CPU Driver → DRAM Received @die:

DQS4 vs. DQ[32:39]



DQS5 vs. DQ[40:47]



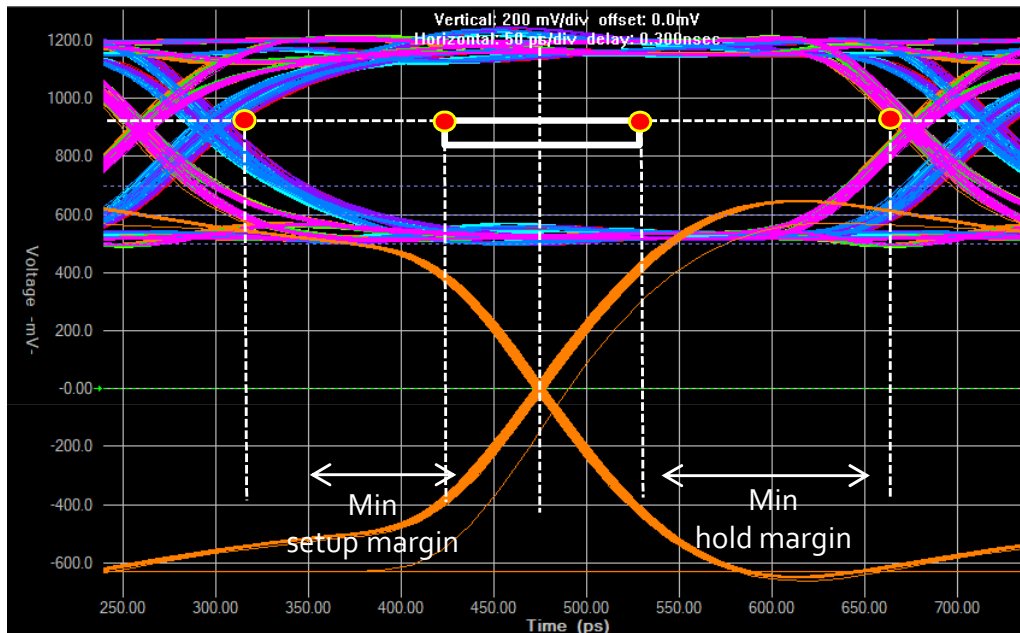
Note:

The purpose of this simulation is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

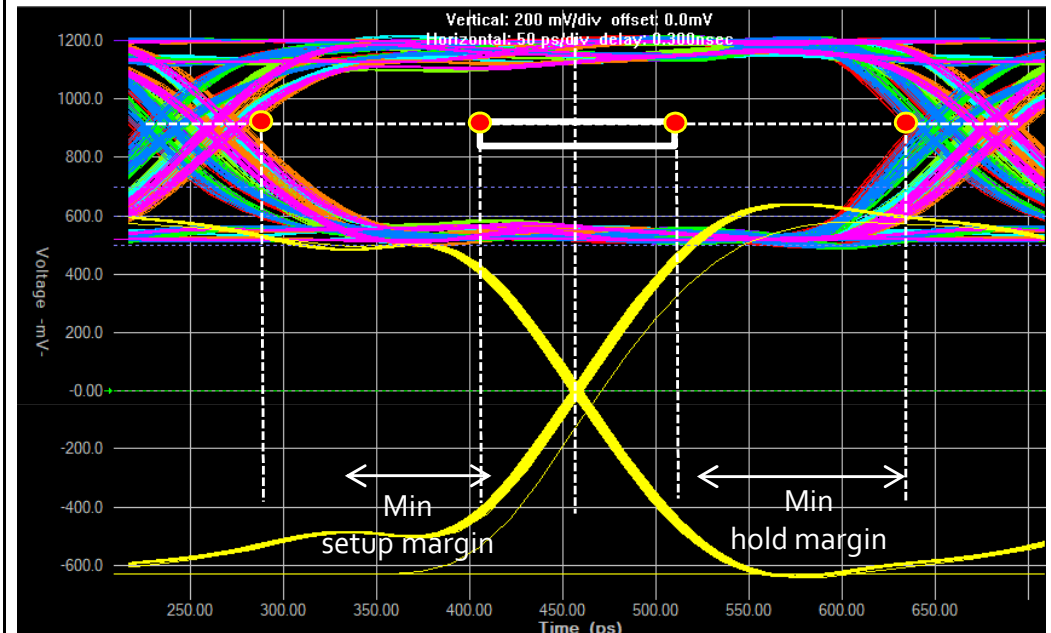
Data Write Simulation Waveform(typ)

CPU Driver → DRAM Received @die:

DQS6 vs. DQ[48:55]



DQS7 vs. DQ[56:63]

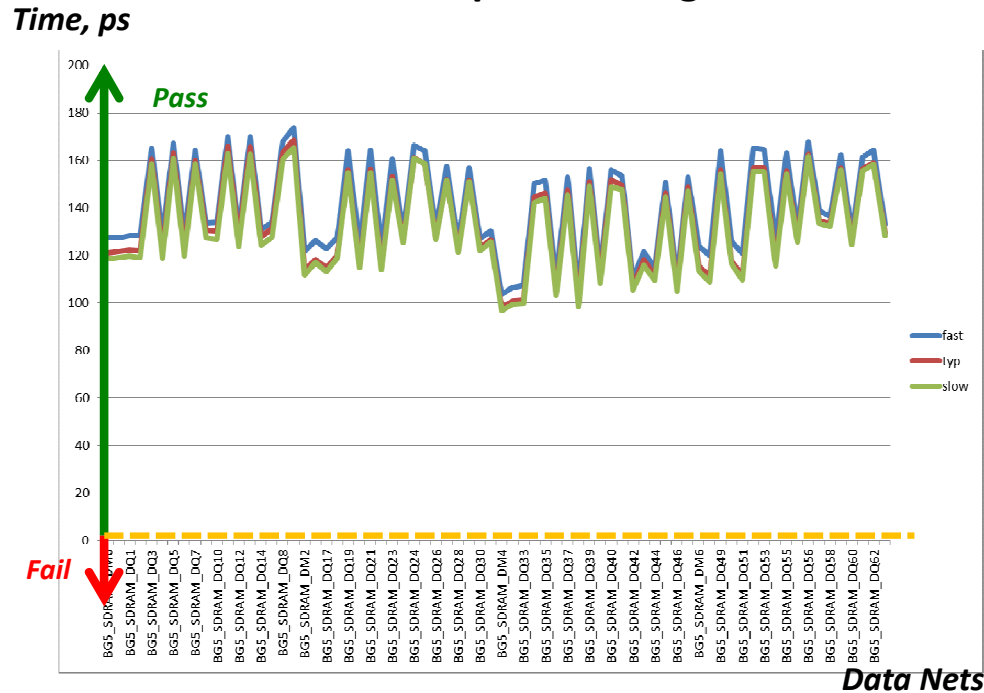


Note:

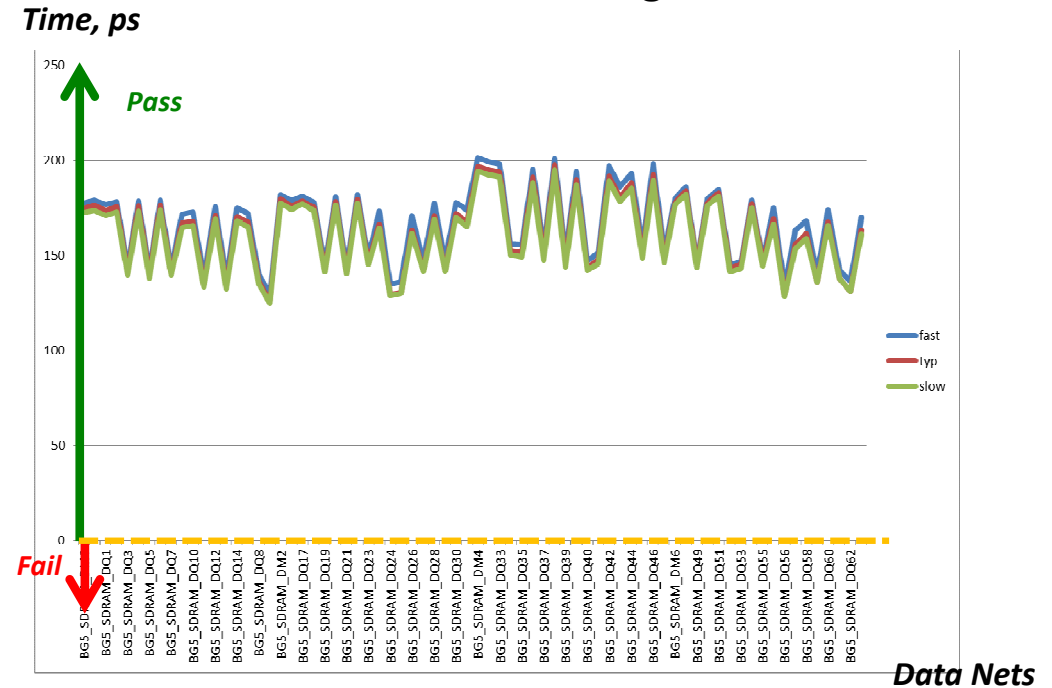
The purpose of this simulation is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

DQS vs. DQ Write Timing Budget

Setup time budget



Hold time budget



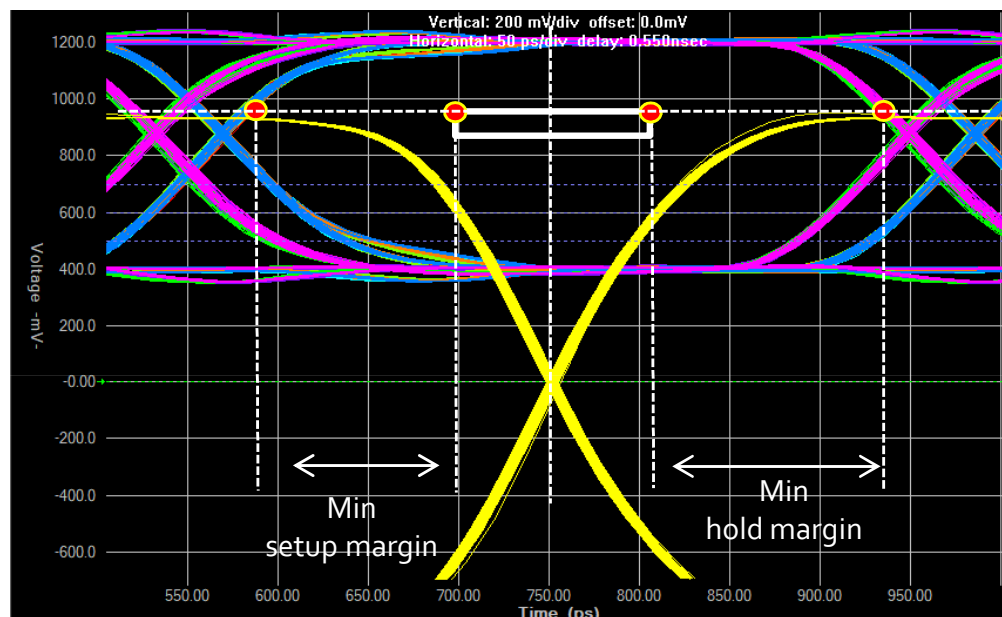
Note:

1. The setup/ hold time criteria are considered the $t_{DS,H(base)}$, $d(t_{DS,H})$ and initial delay δ .
2. Both setup/hold time margin should be positive within specification limit to have enough margin in each nets for pass condition.
3. The simulation include different corners result.

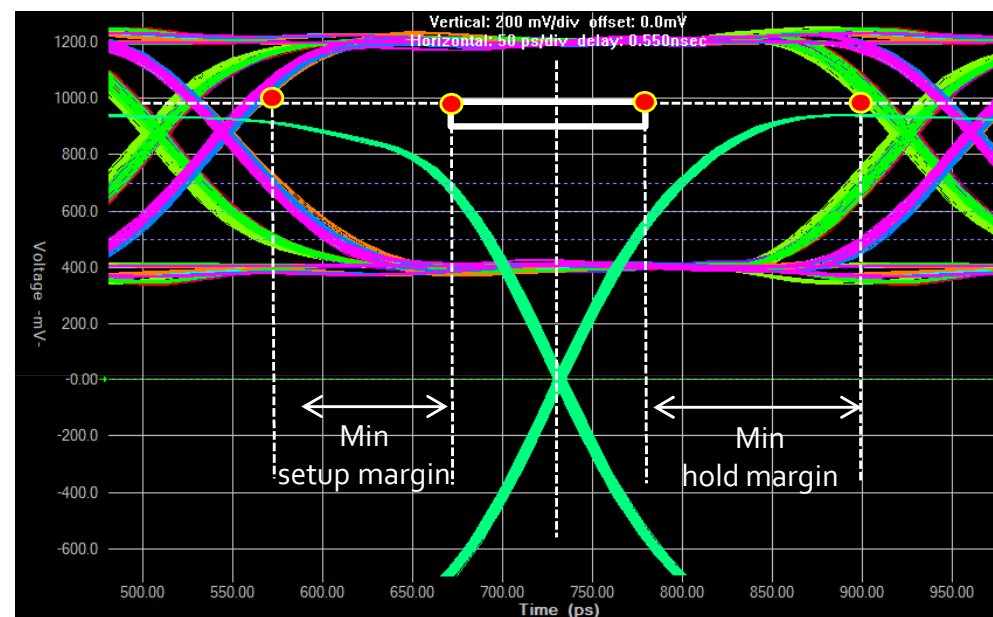
Data Read Simulation Waveform(typ)

DRAM Driver → CPU Received @die:

DQS0 vs. DQ[0:7]



DQS1 vs. DQ[8:15]



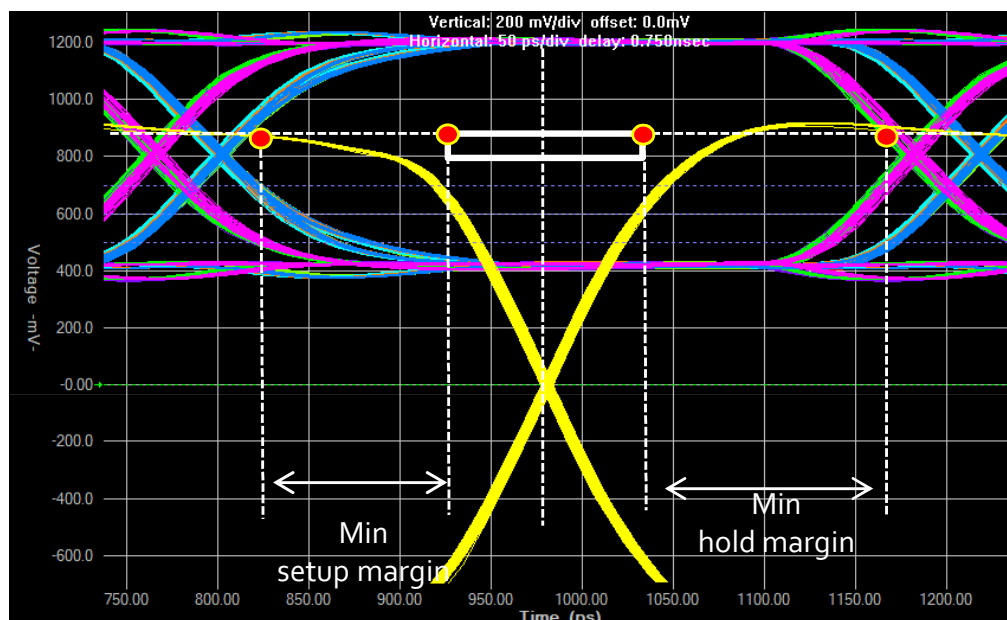
Note:

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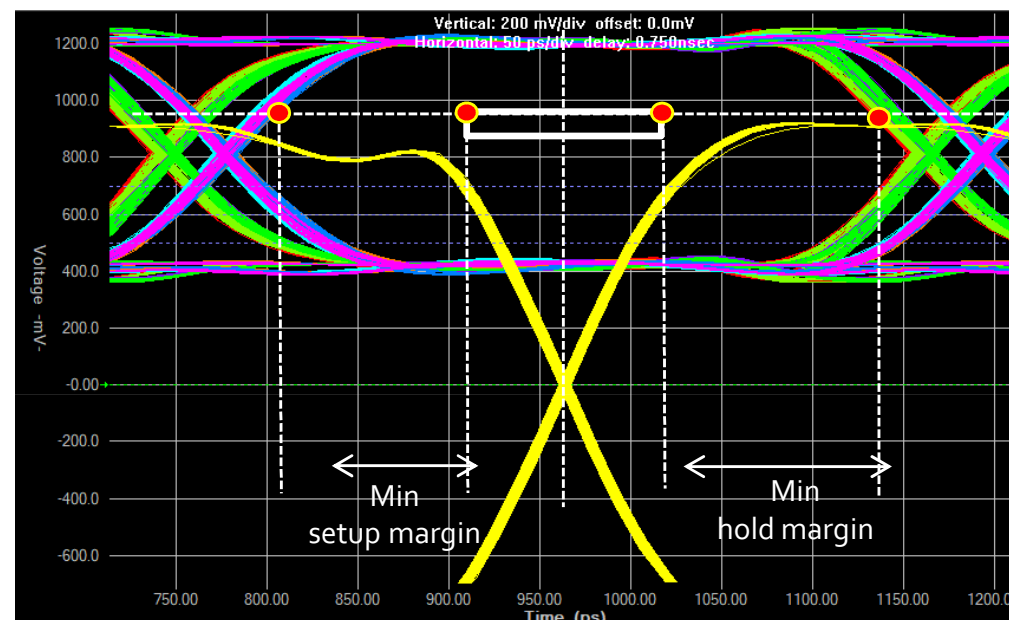
Data Read Simulation Waveform(typ)

DRAM Driver → CPU Received @die:

DQS2 vs. DQ[16:23]



DQS3 vs. DQ[24:31]



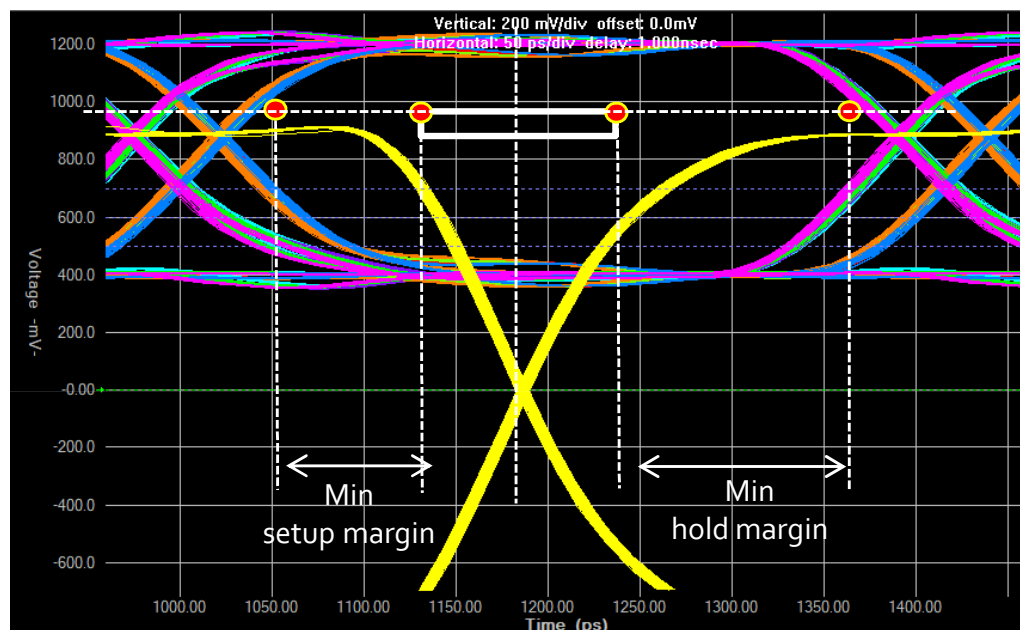
Note:

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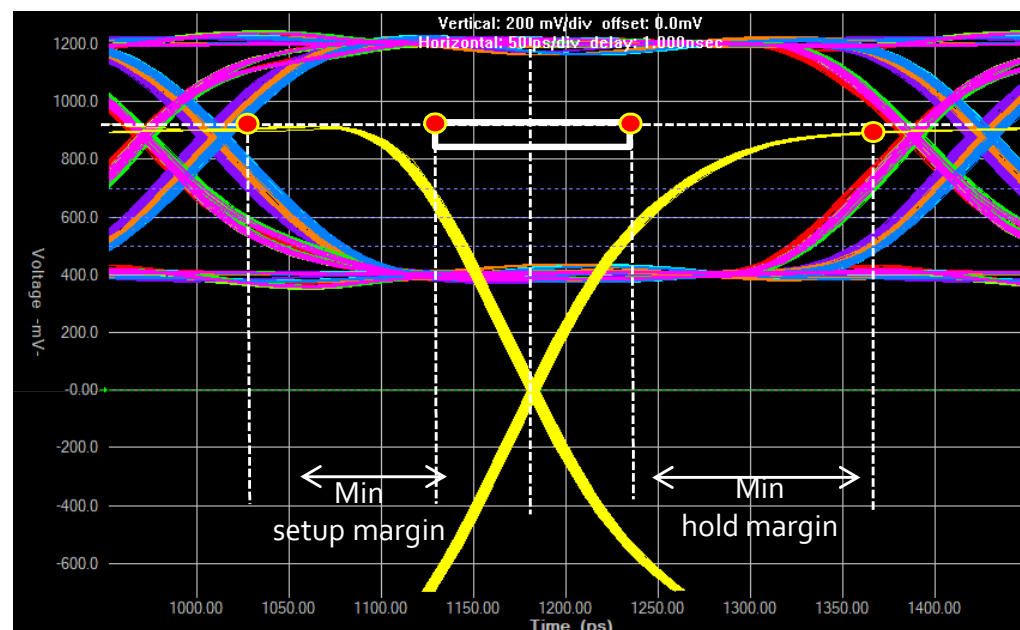
Data Read Simulation Waveform(typ)

DRAM Driver → CPU Received @die:

DQS4 vs. DQ[32:39]



DQS5 vs. DQ[40:47]



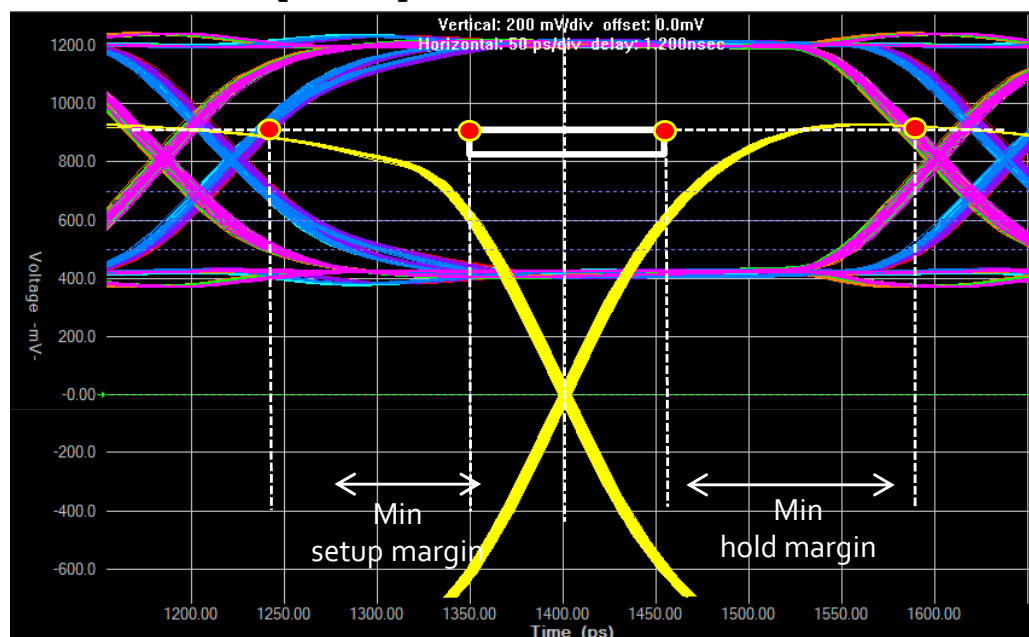
Note:

The purpose of this simulation is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

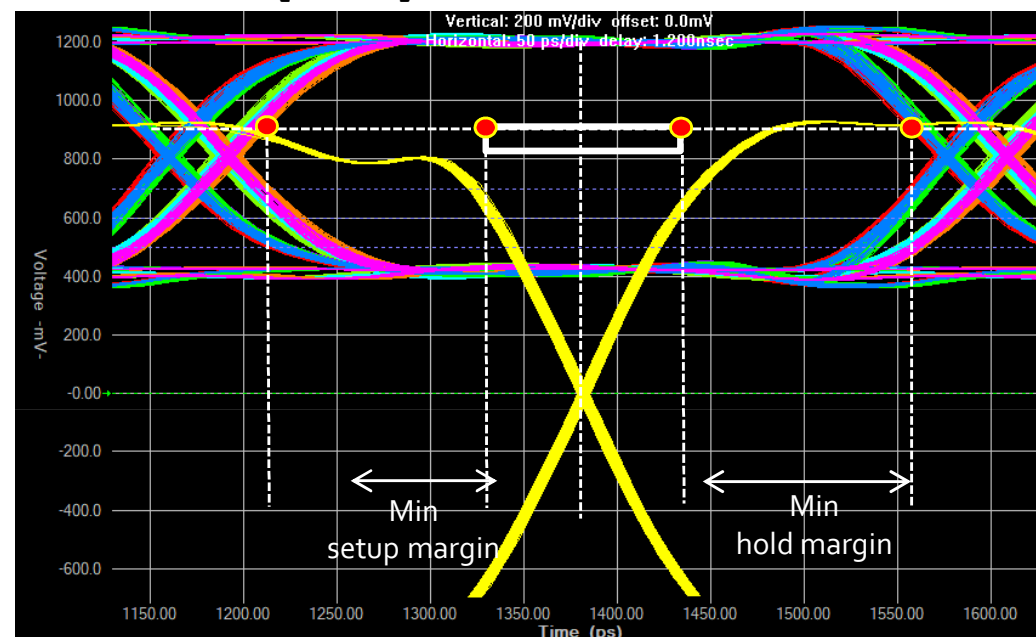
Data Read Simulation Waveform(typ)

DRAM Driver → CPU Received @die:

DQS6 vs. DQ[48:55]



DQS7 vs. DQ[56:63]

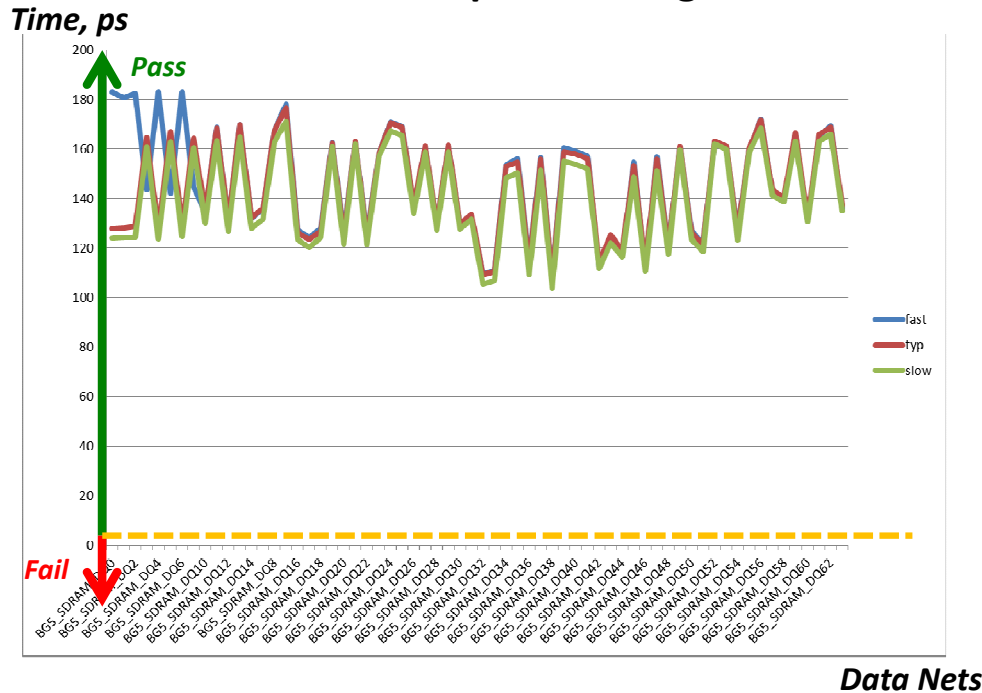


Note:

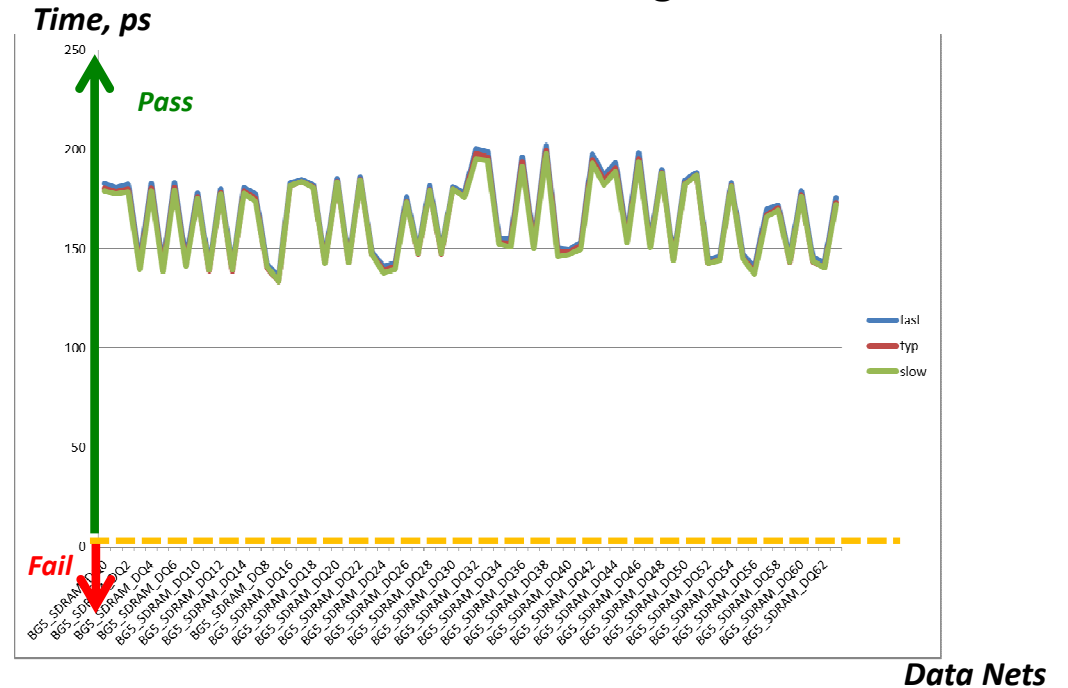
The purpose of this simulation is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

DQS vs. DQ Read Timing Budget

Setup time budget



Hold time budget



Note:

1. The setup/ hold time criteria are considered the $t_{DS,H}(\text{base})$, $d(t_{DS,H})$ and initial delay δ .
2. Both setup/hold time margin should be positive within specification limit to have enough margin in each nets for pass condition.
3. The simulation include different corners result.

Conclusion

- **ADD/CMD :**

The fly-by topology will exist reflection that will cause not enough setup time.

- **DATA :**

1. The data simulation result show enough budget of time margin for pass condition.
2. Suggested to reduce the each DATA group skew and set the constraint in Allegro to control trace length match.

- **The proposed programmable buffers for current design :**

Write Setting (CPU→DRAM)				
Component	Provider	Type	Model	Model Description
CPU	Synaptics	DATA	sgd34ob_12_P120_N60	IO Model with P=120ohm, N=60ohm drive strength
		ADD/CMD	sgd34dfckp_12_P60_N60	IO Model with 60ohm symmetrical drive strength
DRAM	Hynix	DATA	DQ_IN_ODT60	ODT 60ohm
		ADD/CMD	CA_IN	
Read Setting (DRAM→CPU)				
Component	Provider	Type	Model	Model Description
CPU	Synaptics	DATA	sgd34ob_12_PUT60	60ohm ODT
DRAM	Hynix		DQ_DRV34	DQ RON34