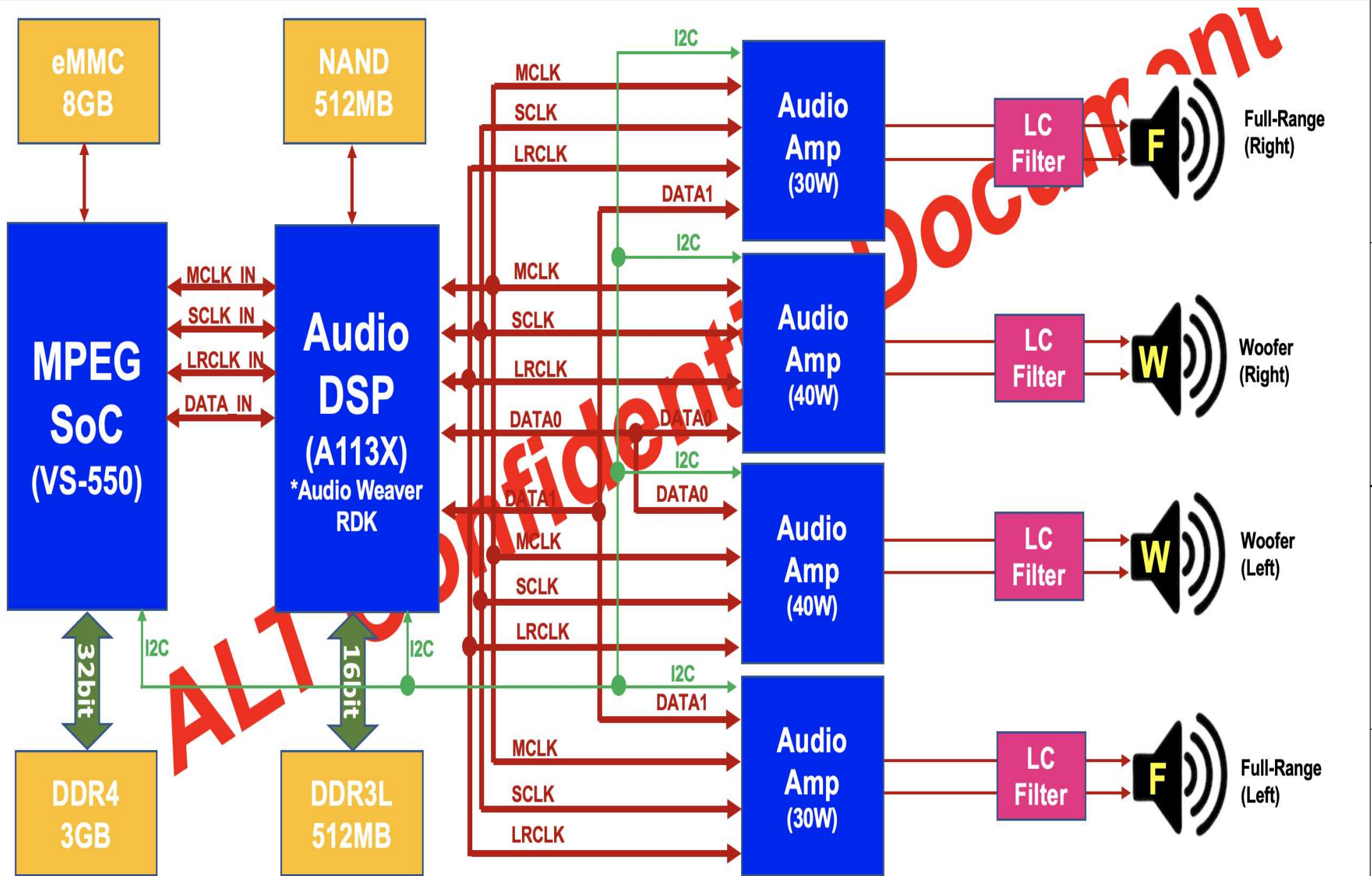
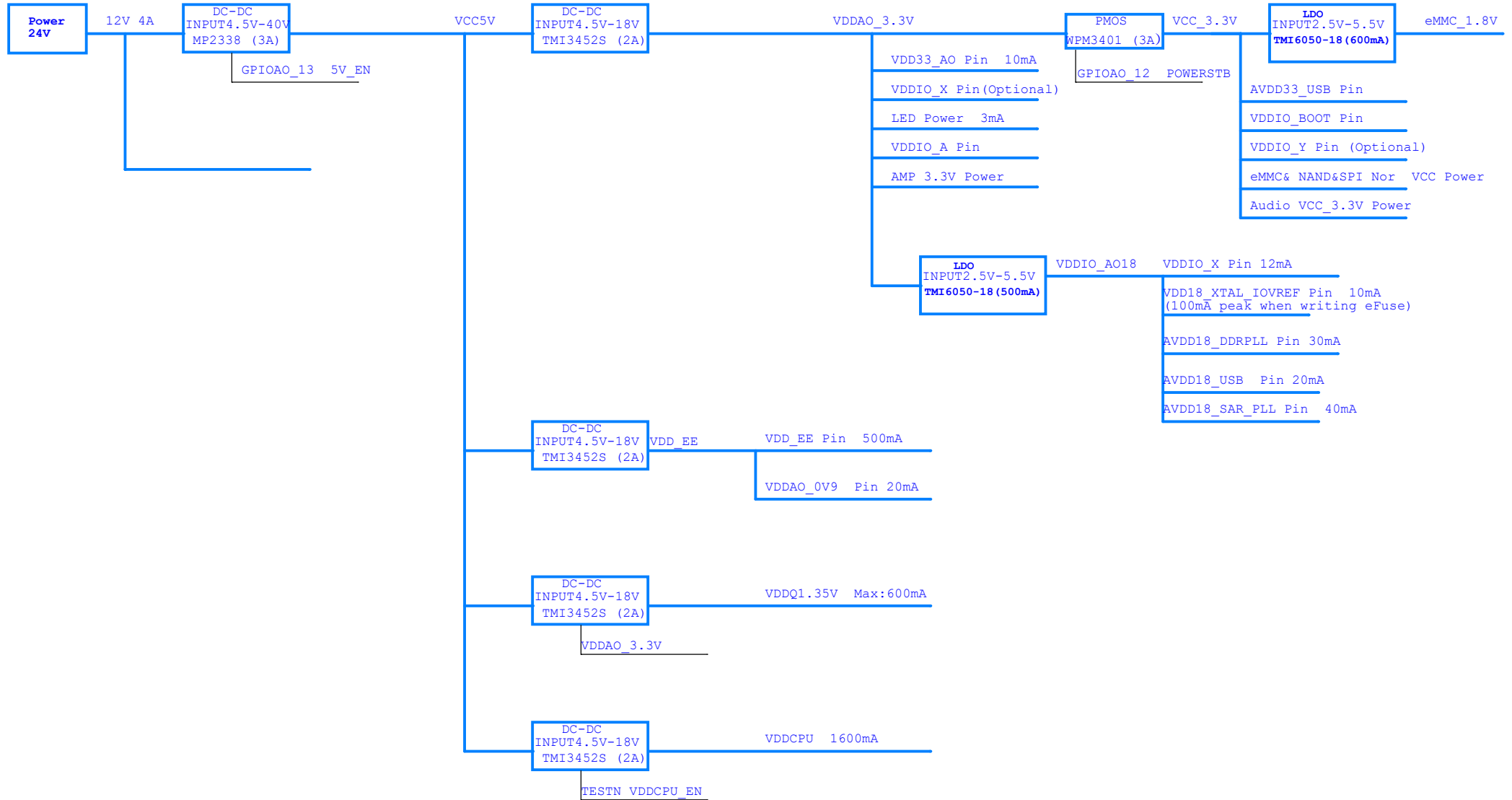
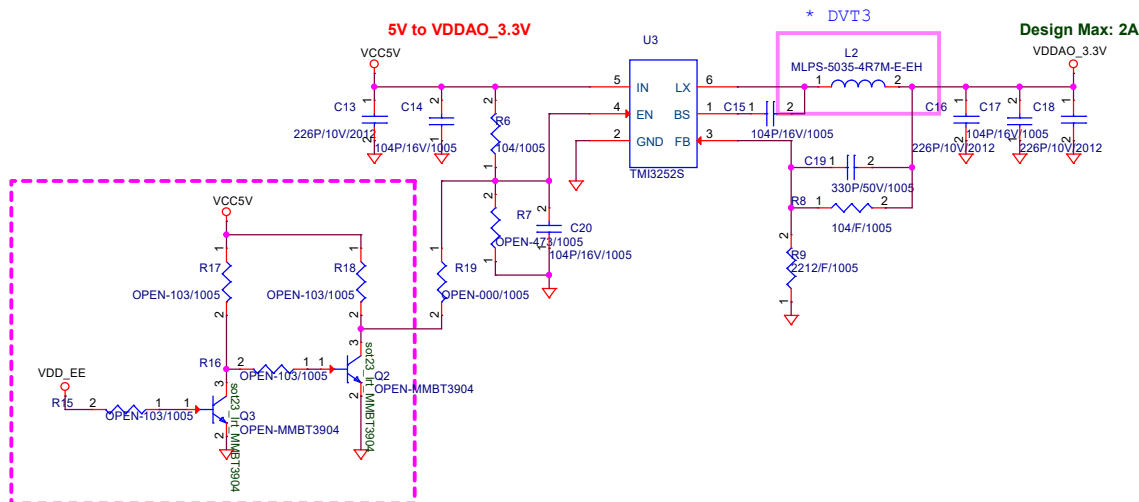
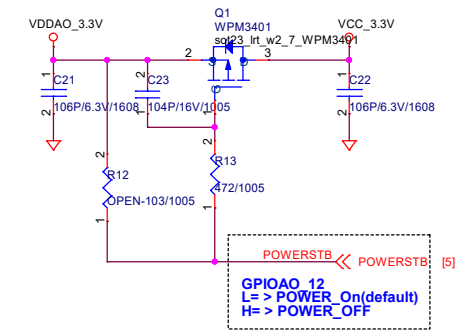
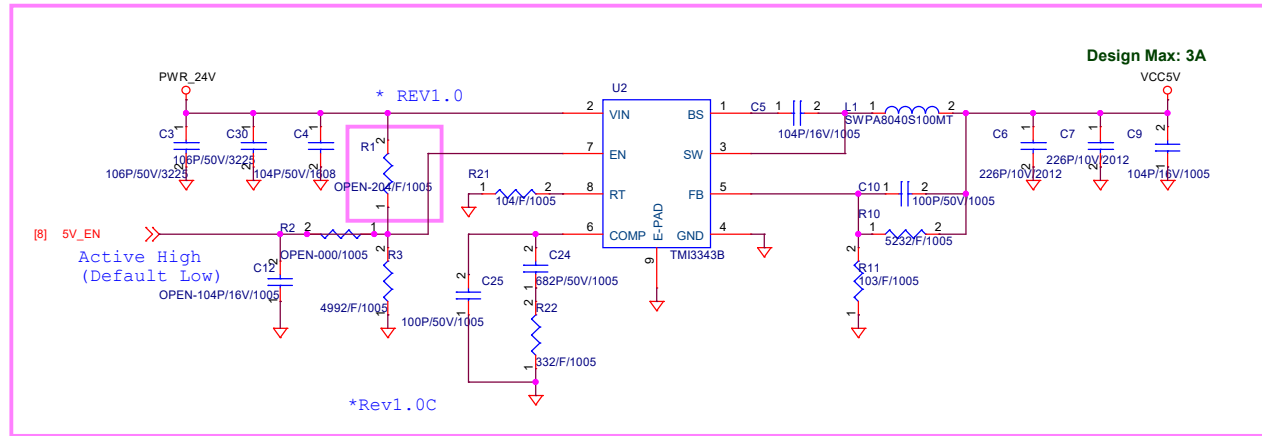
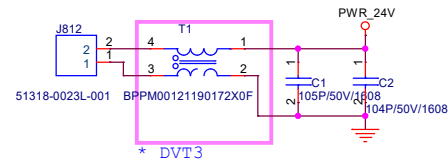
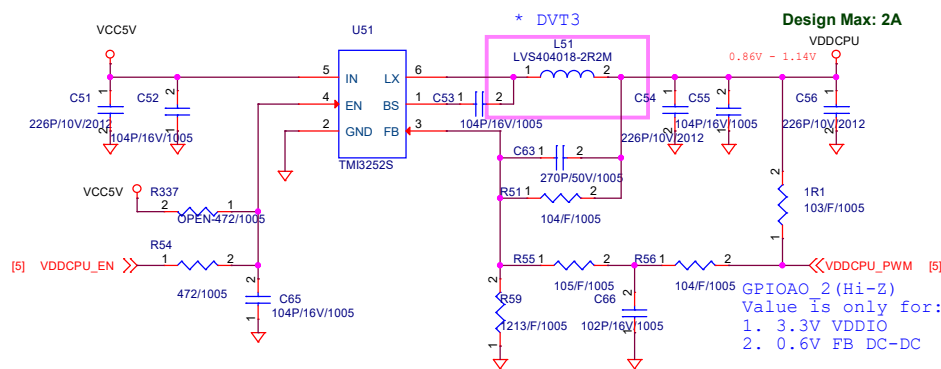




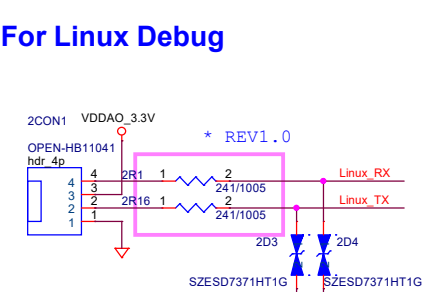
Standby power supply





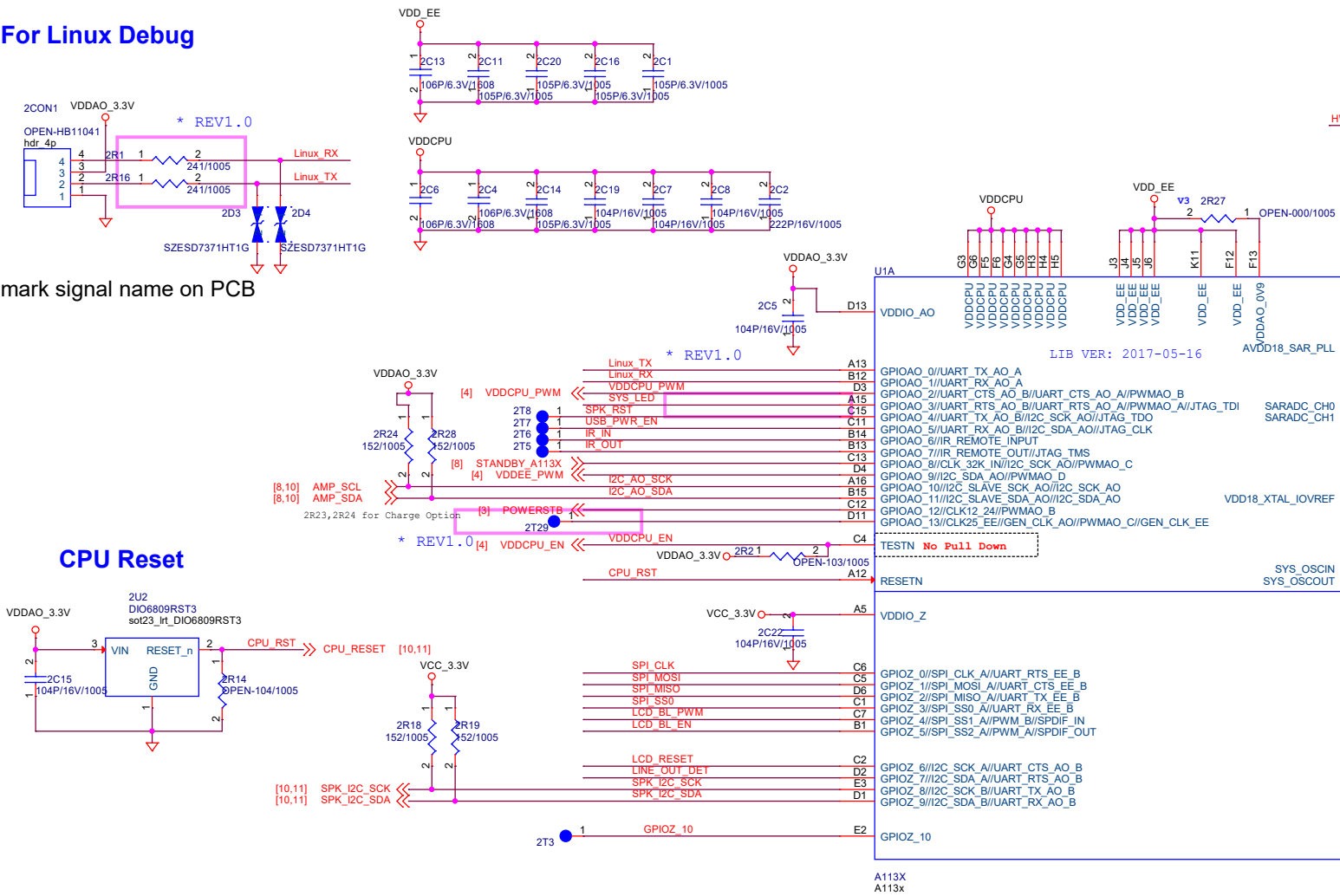


For Linux Debug

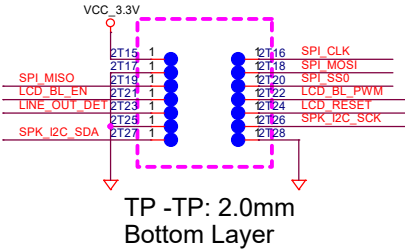


mark signal name on PCB

CPU Reset

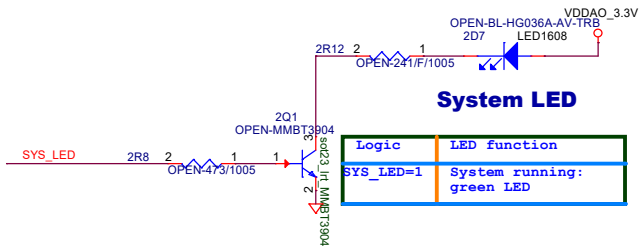


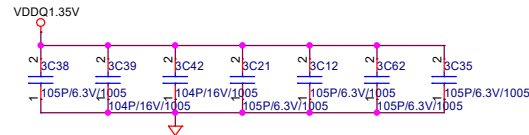
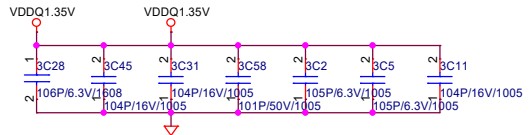
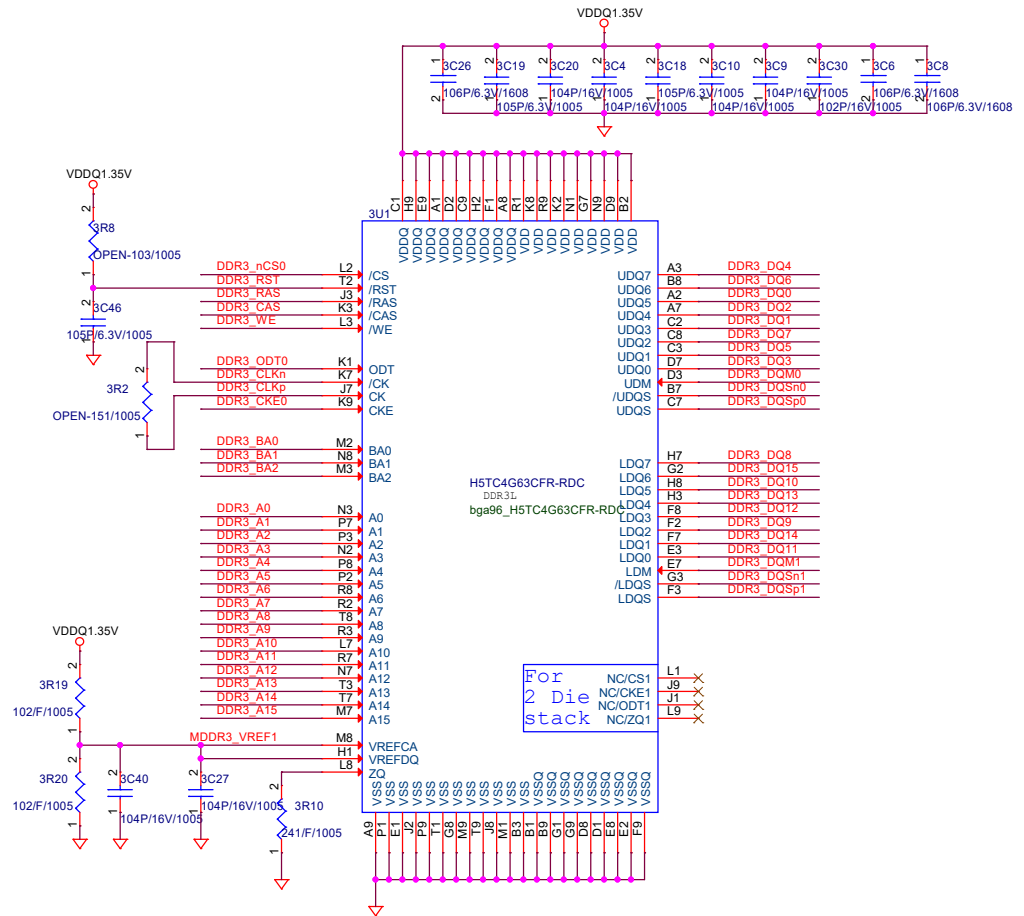
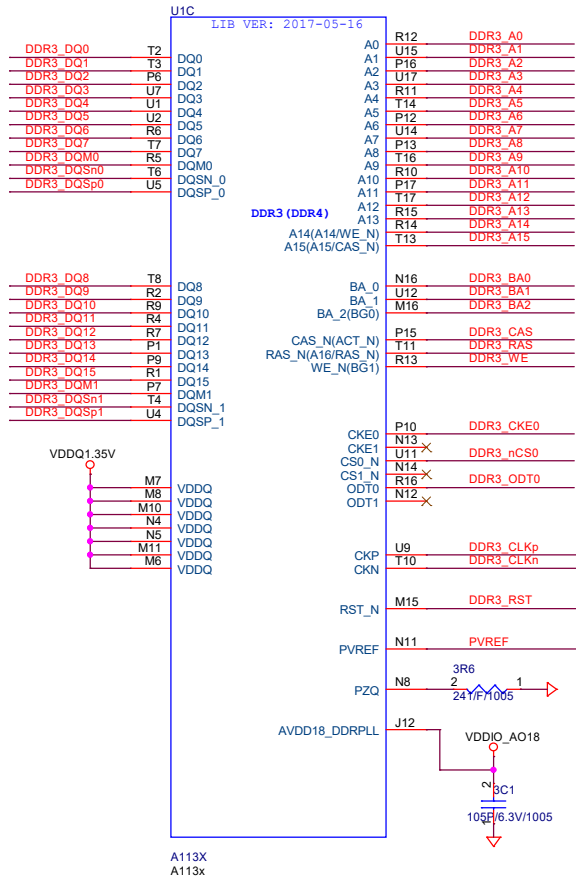
SPI & I2C IO Debug

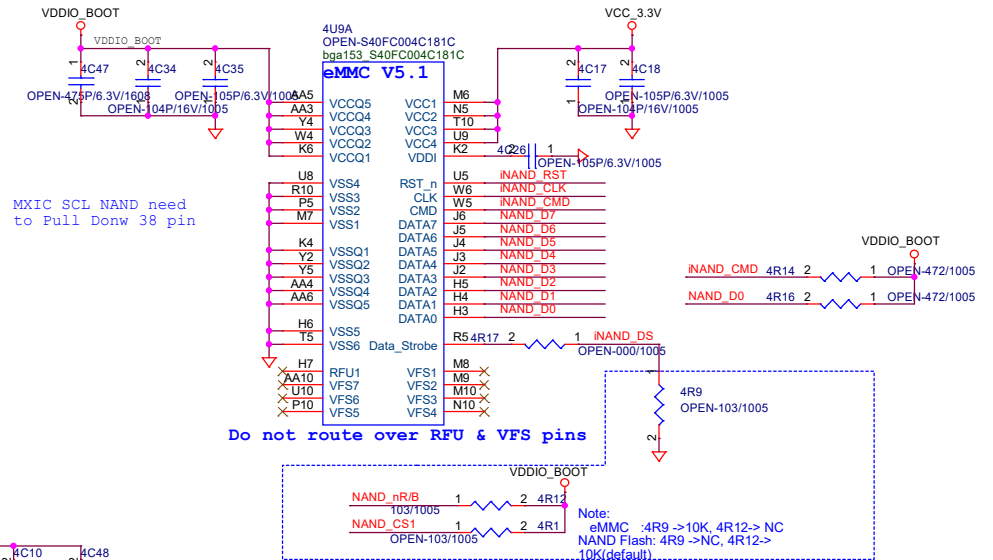
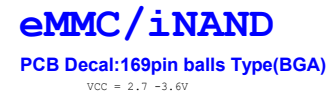


HW ID	0.1	0.2	0.3	1.0	1.1
ADC Data	248	334	420	512	603
PULL-UP	75K	58K	56K	47K	39K
PULL-DOWN	24K	33K	39K	47K	56K
VERSION	O				

System LED







5 NAND (TSOP)

NAND D4 4R52 2 10PEN-472/1005 * REV1.0

NAND D5 4R10 2 172/1005 4K2 TS-1187-1716 10PEN-SW_TS-1187

NAND D6 4R13 2 10PEN-472/1005

NAND D7 4R2 2 10PEN-472/1005

Pinmux diagram for MX30LF4G28AD-TI, showing pin 405 configuration for Normal, Micron ONFI, and Toshiba modes. The diagram includes connections for VCC_3.3V, VDDIO_BOOT, and various NAND flash signals.

Pin 405 Configuration:

- Normal // Micron ONFI // Toshiba:**
 - NC // NC // VCC
 - NC // Vpp// VSS
 - NC//NDI//NC
 - NC // R/B₄ // NC
 - NC // NC // R/B₇ // NC
 - R/B₂
 - R/B₁
 - RE // $\overline{R\overline{E}(W\overline{R})}$ // $\overline{R\overline{E}}$
 - CE₁
 - CE₂
 - NC₂
 - VCC₁
 - VSS₁
 - NC // CE₃ // NC
 - NC // CE₄ // NC
 - CLE
 - ALE
 - $\overline{W\overline{E}}$ // $\overline{W\overline{E}}(\text{CLK})$ // $\overline{W\overline{E}}$
 - WP
 - NC // VSP₃ // NC
 - NC//ENI//NC
 - NC//ENO//NC
 - NC // Vpp// VSS₂
 - NC // NC // VCC₂
- NC // VSSQ // VSS₄**
- NC // VSSQ // VSS₅**
- (I/O14) // VSS**
- (I/O13) // VCCQ**
- I/O₇**
- I/O₆**
- I/O₅**
- I/O₄**
- (I/O12) // VSS**
- NC // VCCQ // PSL**
- NC // VSP₁ // VCCQ**
- VCC₂**
- VSS₂**
- NC // VSP₂(DQS)**
- NC // VCCQ // VCCQ**
- (I/O11) // VSS**
- I/O₃**
- I/O₂**
- I/O₁**
- I/O₀**
- (I/O10) // VCCQ**
- (I/O₉) // VSS**
- (I/O₈) // NC**
- VSS₃**

Connections:

- VCC_3.3V** (Pin 1, 2, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24)
- VDDIO_BOOT** (Pin 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100)
- NAND nR/B** (Pin 7)
- NAND nRE** (Pin 8)
- NAND CS1** (Pin 9)
- NAND CLE** (Pin 16)
- NAND ALE** (Pin 17)
- NAND nWE** (Pin 18)
- WpN** (Pin 19)
- NAND D7** (Pin 48)
- NAND D6** (Pin 49)
- NAND D5** (Pin 50)
- NAND D4** (Pin 51)
- NAND PSL** (Pin 52)
- NAND VSP** (Pin 53)
- NAND D3** (Pin 61)
- NAND D2** (Pin 62)
- NAND D1** (Pin 63)
- NAND D0** (Pin 64)

MX30LF4G28AD-TI (Pin 405)

isp48_w20 (Pin 405)

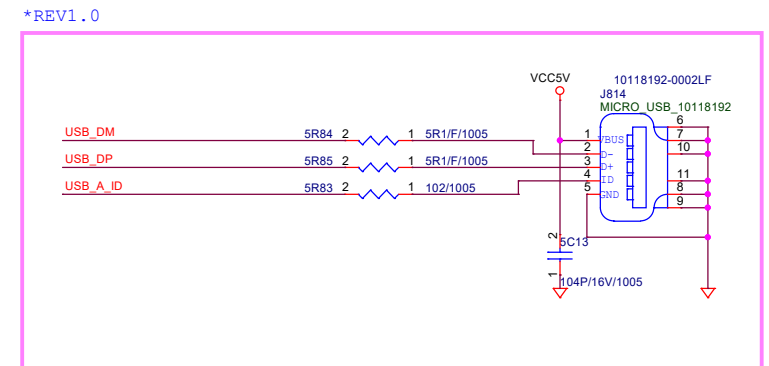
MX30LF4G28AD-TI (Pin 405)

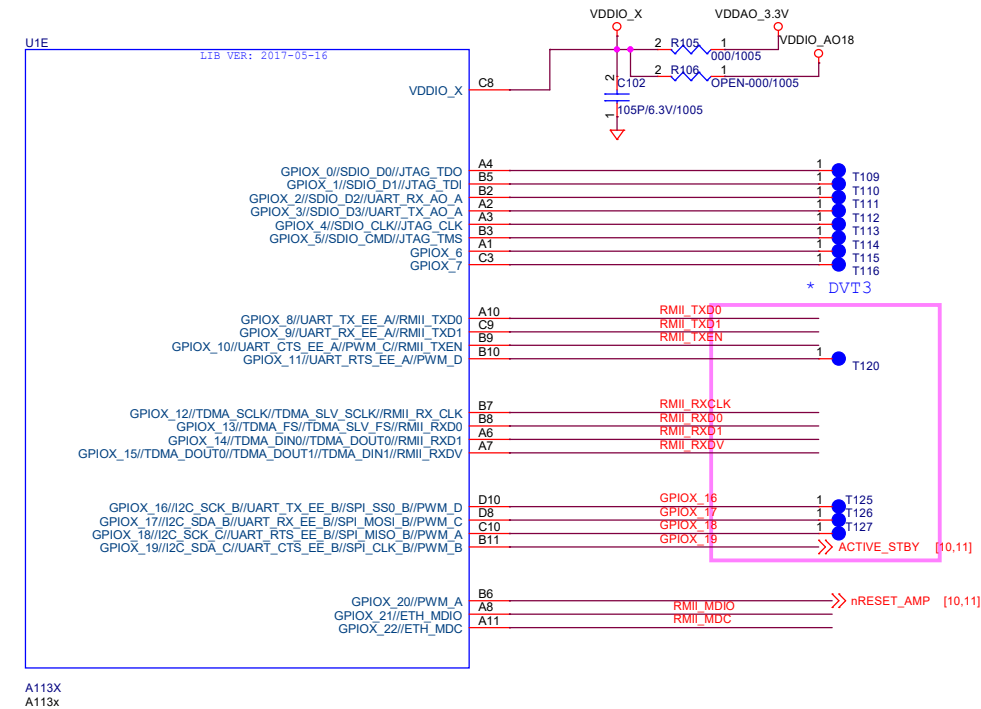
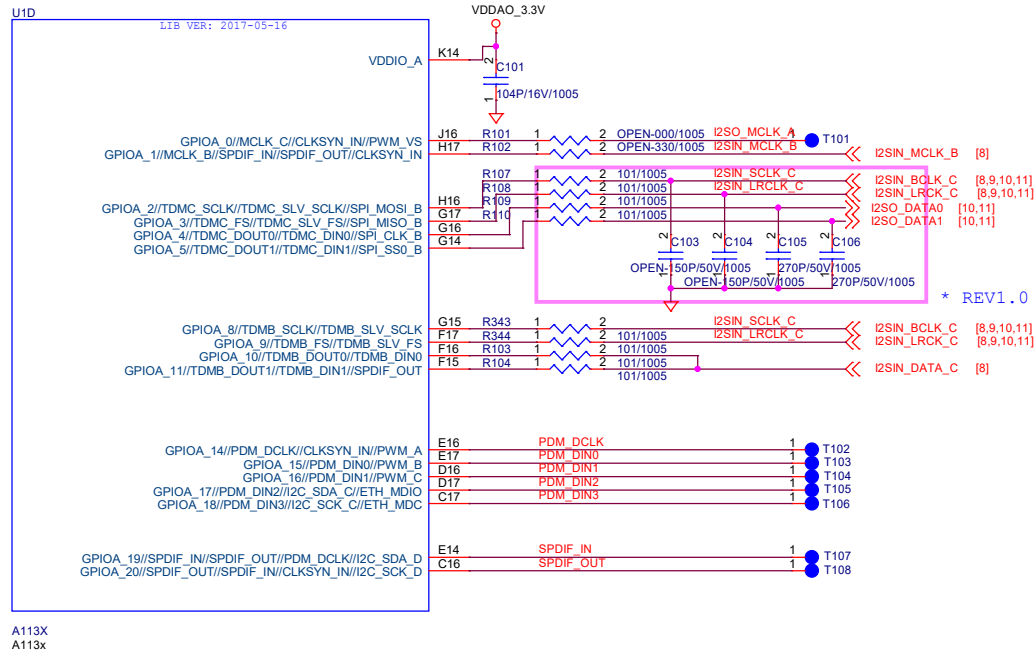
The schematic shows the VDDIO_BOOT pin configuration. The pin is connected to VDDIO_BOOT, has a 4R4 pull-up resistor to VDDIO_BOOT, a 4C9 capacitor to ground, and a 4R7 pull-down resistor to ground. The pin is also connected to the NAND_PSL and NAND_VSP pins of the NAND controller.

eMMC NC PIN FOR ALLEGRO

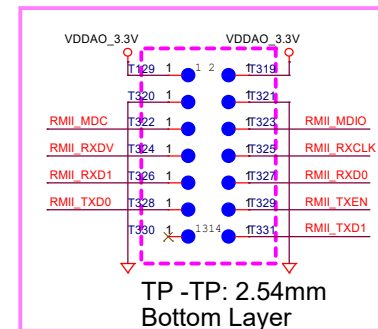


			
Title			
07. A113X_FLASH			
Size A3	Document Number		Rev
	A12 MAX-AMP B/D		0.31
Date:	Wednesday, October 27, 2021	Sheet 7 of 11	

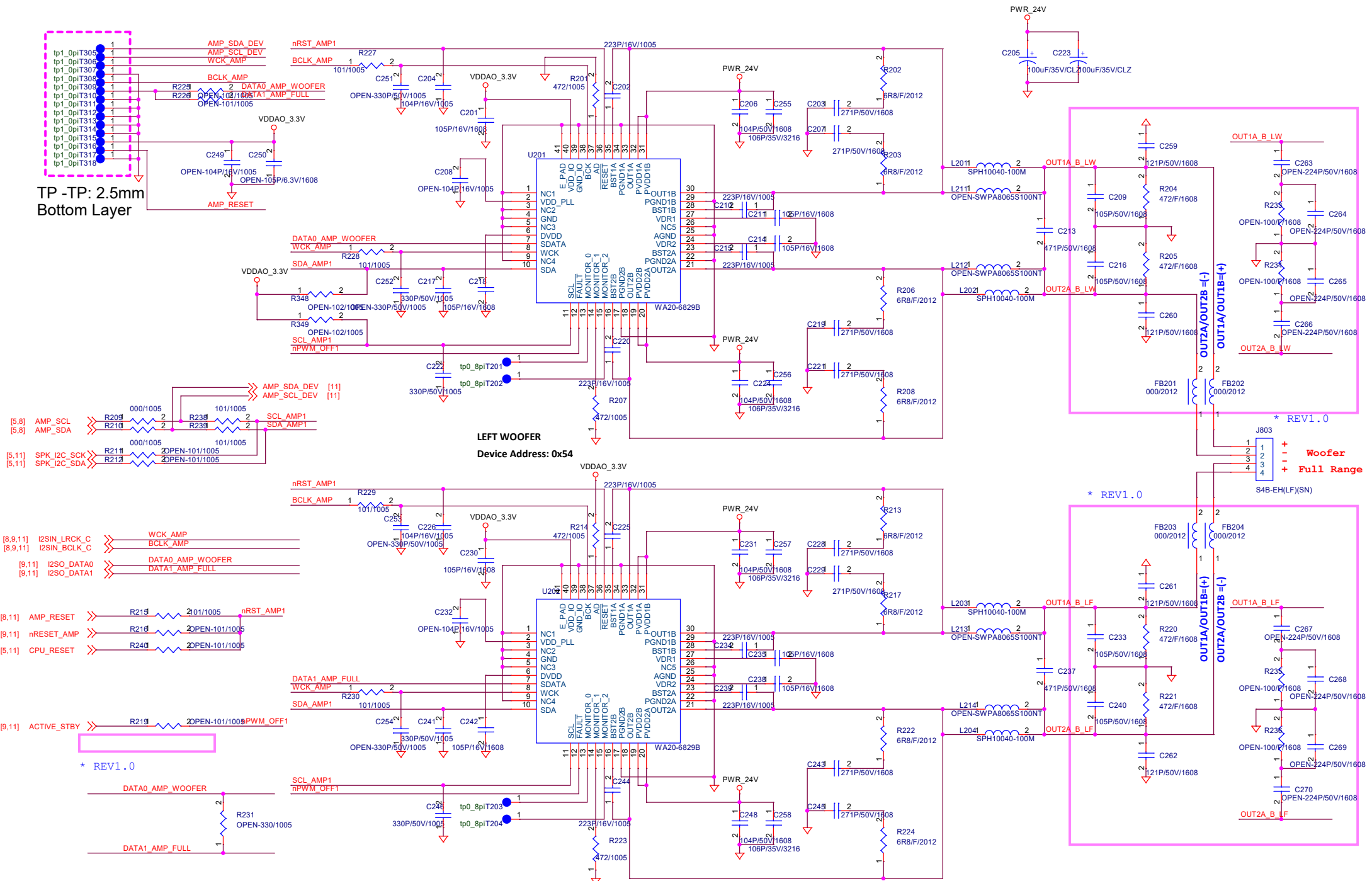




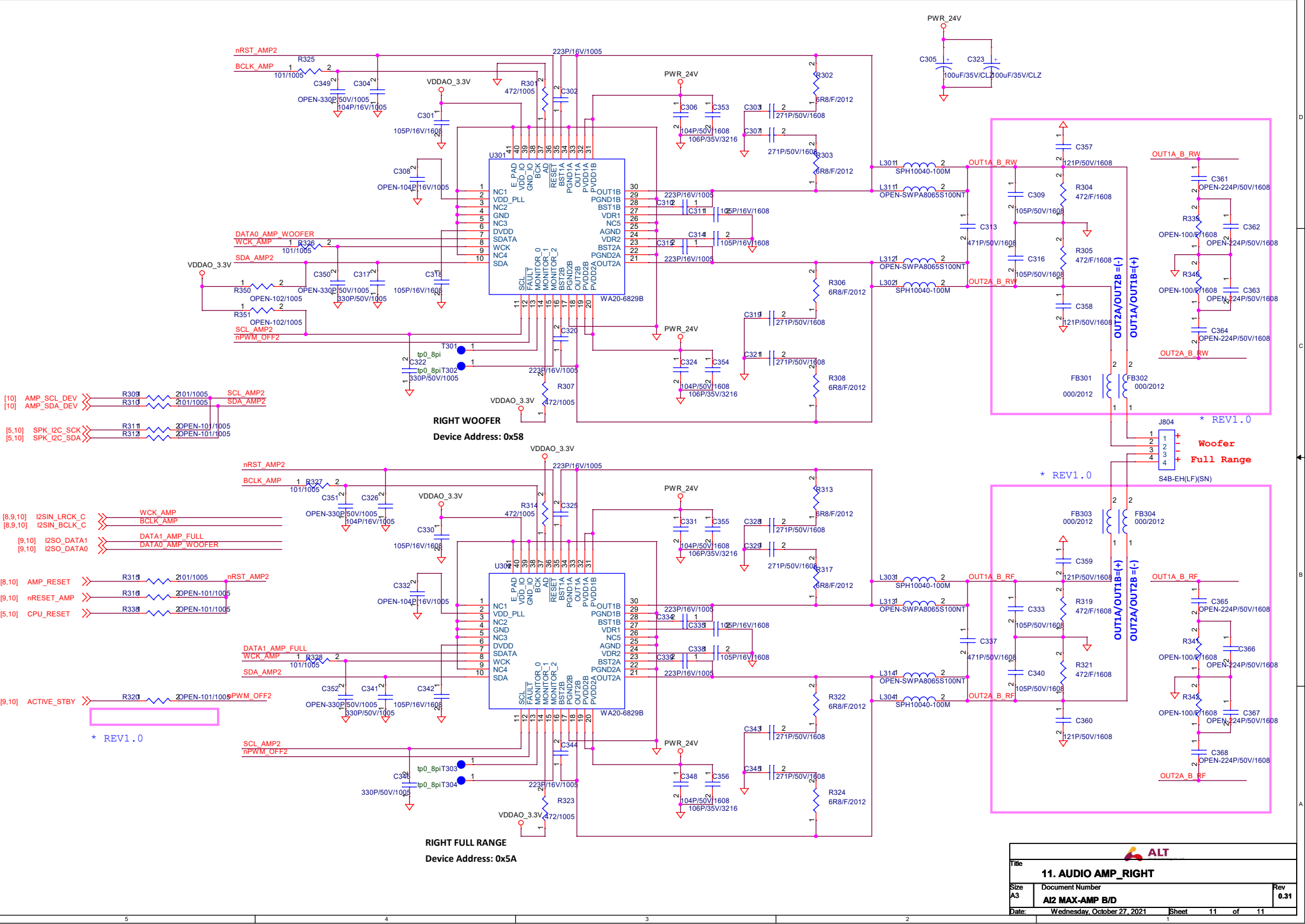
* DVT3



TP -TP: 2.5mm
Bottom Layer



10. AUDIO AMP_LEFT		
Size A3	Document Number A12 MAX-AMP B/D	Rev 0.31
Date: Wednesday, October 27, 2021	Sheet 10 of 11	



Title			11. AUDIO AMP_RIGHT
Size	Document Number	Rev	
A3	A12 MAX-AMP B/D	0.31	
Date:	Wednesday, October 27, 2021	Sheet	11 of 11