

## 4.5 W Boosted Digital Speaker Amplifier with Feedback-Loop

### Features

- High Efficiency Boost Converter
  - Typical output voltage 10 V
  - Multi-step Class-H boost control to maximize efficiency
- High Performance Digital Speaker Amplifier
  - Full digital Class-D audio amplifier
  - Max. 6.0 W<sup>1)</sup> at 8 Ω, THD+N < 1%, 1 kHz
  - SNR 105 dB, THD+N 0.01%
  - Idle noise < 8.5 μV<sub>RMS</sub> at the receiver mode
  - Standby Power < 50uW
  - Low idle power consumption with noise gate
  - Digital audio input interface (I<sup>2</sup>S / 8ch-TDM)
  - Support four I<sup>2</sup>C addresses with a single pin
  - SDO output high impedance control for stereo speakers
- Digital Signal Processing for Sound Tuning
  - Soft volume and soft mute
  - Dynamic range compressor and high pass filter
  - Post scaler
  - Digital audio feedback signal for echo cancelation
- Protections
  - Overcurrent protection
  - Under voltage protection
  - Overvoltage protection for boost converter
  - Overcurrent limit for boost converter
  - Thermal management / shutdown circuit
- Others
  - Fault diagnostics by I<sup>2</sup>C interface
  - Input clock monitoring circuit with internal oscillator

- Internal low power, low noise PLL
- Supports four channel applications
- SmartPowerMeter™: monitoring output for thermal status

### Applications

- Mobile Phones
- Tablets
- Wireless Mobile Speakers

### Description

This document contains the detailed specifications of the SMA1857 digital Class-D audio amplifier with an integrated boost converter. From a single cell Li-ion battery power supply, the boost converter converts boosted output voltage into a full digital amplifier to make the stable large sound pressure levels.

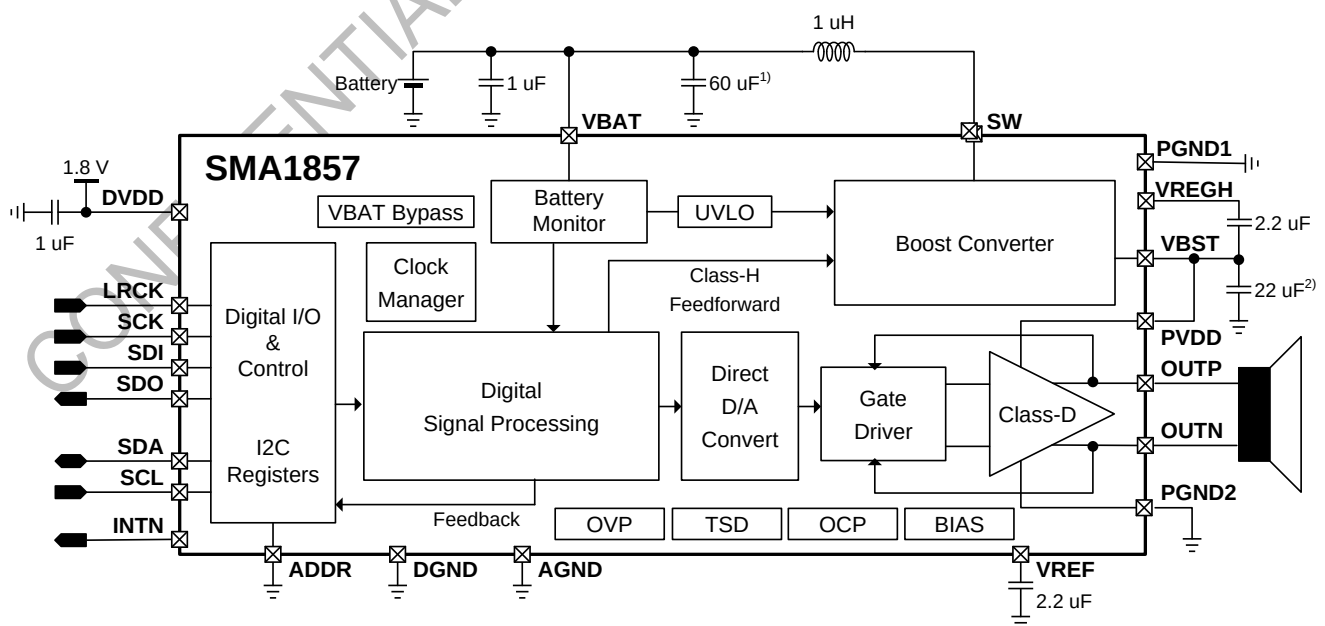
### Device Information

| Part Number | Package       | Body Size         |
|-------------|---------------|-------------------|
| SMA1857-W   | 4 x 6 - WLCSP | 1.67 mm x 2.47 mm |

#### Note

- 1) Analog Gain 17.9dB (SPK Mode x3.6) and it depends on the thermal condition of the boards.

### Simplified Block Diagram



### **Notes**

- 2) The typical value is 22  $\mu\text{F}$  if a battery is connected.  
If there is no battery at the boost converter input, the total capacitance should be over 60  $\mu\text{F}$ .
- 3) The typical value is 22  $\mu\text{F}$  to 33  $\mu\text{F}$ . The minimum capacitance at 10 V derating is 3  $\mu\text{F}$ .

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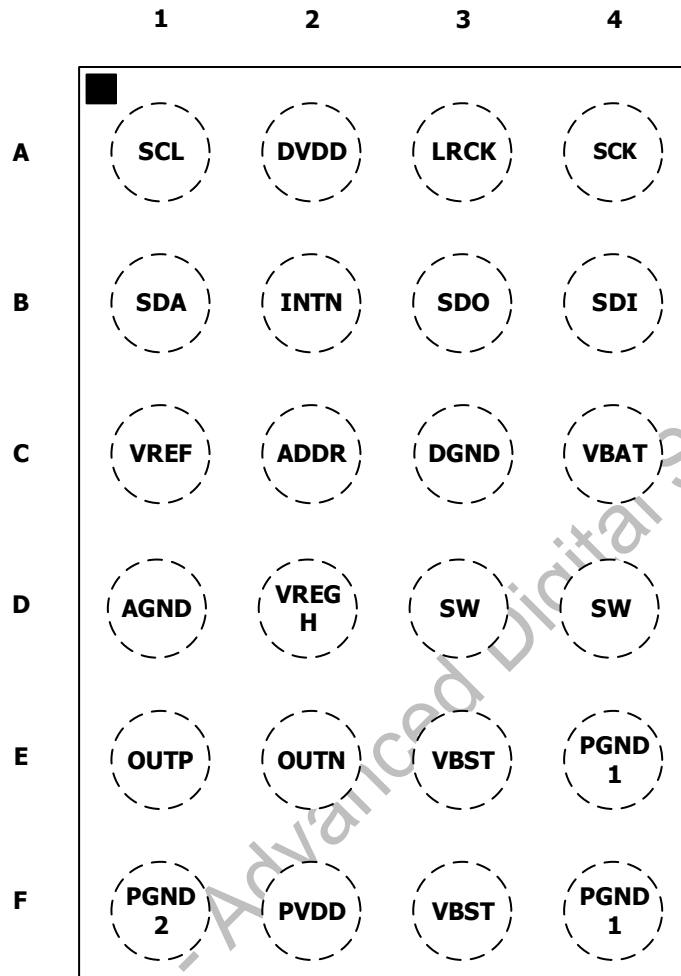
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**Pin Assignments**

Top View



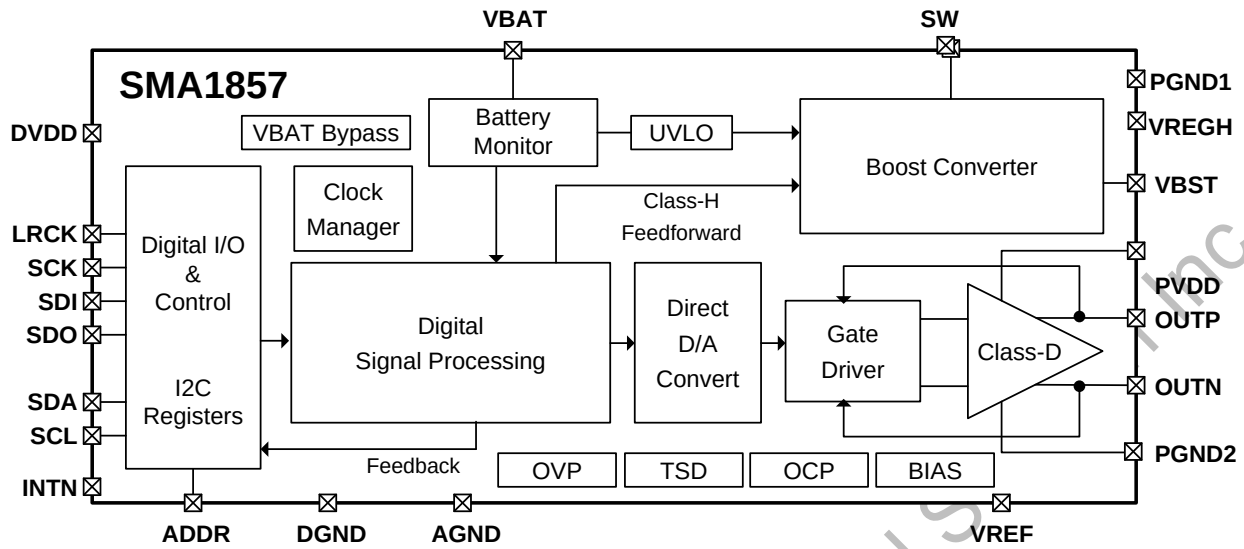
24 Pin, 1.67 mm x 2.47 mm x 0.622 mm, 0.4 Pitch – WLCSP

**Pin Description**

| WLCSP | Name  | I/O | Description                                                                                                                | Power Rail |
|-------|-------|-----|----------------------------------------------------------------------------------------------------------------------------|------------|
| A1    | SCL   | I   | I <sup>2</sup> C Serial Clock                                                                                              | DVDD       |
| A2    | DVDD  | P   | Digital Power Supply and I/O Power Supply                                                                                  | DVDD       |
| A3    | LRCK  | I   | I <sup>2</sup> S Left-Right Clock                                                                                          | DVDD       |
| A4    | SCK   | I   | I <sup>2</sup> S Serial Clock                                                                                              | DVDD       |
| B1    | SDA   | I/O | I <sup>2</sup> C Serial Data                                                                                               | DVDD       |
| B2    | INTN  | O   | Interrupt Output (open-drain output and a pull-up resistor is needed.)                                                     | DVDD       |
| B3    | SDO   | O   | I <sup>2</sup> S Serial Data Output                                                                                        | DVDD       |
| B4    | SDI   | I   | I <sup>2</sup> S Serial Data Input                                                                                         | DVDD       |
| C1    | VREF  | I/O | Speaker Reference                                                                                                          | VBAT       |
| C2    | ADDR  | I   | I <sup>2</sup> C Address Selection (see the I <sup>2</sup> C table – adjustable to one of four I <sup>2</sup> C addresses) | DVDD       |
| C3    | DGND  | G   | Digital Ground                                                                                                             | DVDD       |
| C4    | VBAT  | P   | Battery Supply                                                                                                             | VBAT       |
| D1    | AGND  | G   | Analog Ground                                                                                                              | VBAT       |
| D2    | VREGH | P   | High Side Gate Driver's Supply $V_{REGH} = V_{BST} - V_{BAT}$                                                              | PVDD       |
| D3    | SW    | I   | Boost Converter Switch                                                                                                     | PVDD       |
| D4    | SW    | I   | Boost Converter Switch                                                                                                     | PVDD       |
| E1    | OUTP  | O   | Positive Output Driver                                                                                                     | PVDD       |
| E2    | OUTN  | O   | Negative Output Driver                                                                                                     | PVDD       |
| E3    | VBST  | P   | Boost Converter Output Voltage                                                                                             | PVDD       |
| E4    | PGND1 | G   | Power Ground for Boost Converter                                                                                           | PVDD       |
| F1    | PGND2 | G   | Power Ground for Class-D Amplifier                                                                                         | PVDD       |
| F2    | PVDD  | P   | Class-D Amplifier Power Supply                                                                                             | PVDD       |
| F3    | VBST  | P   | Boost Converter Output Voltage                                                                                             | PVDD       |
| F4    | PGND1 | G   | Power Ground for Boost Converter                                                                                           | PVDD       |

\*P: Power, G: Ground, O: Output, I: Input, I/O: Bidirectional

**Functional Diagram**



**Absolute Maximum Ratings**

Stress(es) beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only. It does not imply the functional operation of the device or other conditions beyond those is indicated in the following. Exposure to absolute maximum rating condition(s) for extended periods may affect device reliability.

| Parameter                                                                       | Lower Limit | Upper Limit | Unit |
|---------------------------------------------------------------------------------|-------------|-------------|------|
| Battery Supply Voltage (VBAT) to AGND <sup>1)</sup>                             | -0.3        | 6.0         | V    |
| Digital & I/O Supply Voltage (DVDD) to DGND <sup>1)</sup>                       | -0.3        | 2.1         | V    |
| Boosted Output Voltage (VBST) to PGND1 <sup>1)</sup>                            | -0.3        | 12.5        | V    |
| Class-D Amplifier Supply Voltage (PVDD) to PGND2 <sup>1)</sup>                  | -0.3        | 12.5        | V    |
| Boost Switch Voltage (SW) <sup>3)</sup>                                         | -0.3        | 12.5        | V    |
| Class-D Amplifier Output Voltage (OUTP, OUTN) to PGND2 <sup>1)</sup>            | -0.3        | 12.5        | V    |
| Digital I/O Voltage (SCK, LRCK, SDO, SDI, SCL, SDA, ADDR) to DGND <sup>1)</sup> | -0.3        | DVDD + 0.3  | V    |
| Human Body Model (HBM) ESD <sup>2)</sup>                                        | -2000       | 2000        | V    |
| Charged Device Model (CDM) ESD                                                  | -800        | 800         | V    |
| Operating Ambient Temperature                                                   | -40         | 85          | °C   |
| Operating Junction Temperature                                                  | -40         | 150         | °C   |
| Storage Ambient Temperature                                                     | -65         | 150         | °C   |
| Lead Soldering Temperature (within 10 sec)                                      |             | 300         | °C   |

**Notes**

- 1) GND: all AGND, DGND, PGND1, and PGND2 should be within the limit.
- 2) HBM per JESD22-A114 for all pins
- 3) Using demo board, with 1 GHz differential active probe on SW pin, AC pulses between -1.5 V and +14 V can be observed without damaging the device, as these spikes do not end up inside the actual device.

**Thermal Characteristic**

| Parameter                                                     | Symbol        | Value | Unit |
|---------------------------------------------------------------|---------------|-------|------|
| Thermal Resistance Junction to Ambient <sup>1) &amp; 2)</sup> | $\Theta_{JA}$ | 59.3  | °C/W |

**Notes**

- 1)  $T_A = 25\text{ °C}$  for WLCSP package
- 2) Measured in still air-free convection condition (conforms to JESD51-2A) on high effective thermal conductivity JESD51-6, JESD51-8 with 4-layer test board

**Recommended Operating Conditions**

| Parameter                      | Symbol     | Min. | Typ. | Max. | Unit |
|--------------------------------|------------|------|------|------|------|
| Battery Supply Voltage         | $V_{BAT}$  | 2.8  | 3.6  | 5.5  | V    |
| Digital and I/O Supply Voltage | $V_{DVDD}$ | 1.65 | 1.8  | 1.95 | V    |

**Electrical Characteristics - DC**

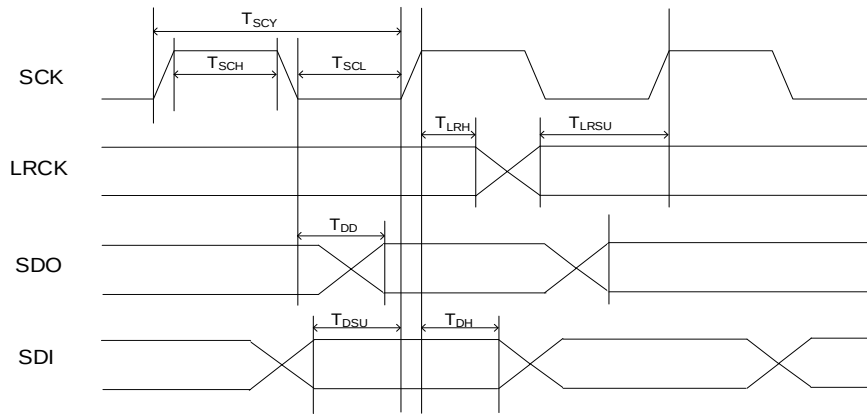
$V_{BAT} = 3.6\text{ V}$ ,  $V_{DVDD} = 1.8\text{ V}$ ,  $V_{BST} = 10.0\text{ V}$ ,  $f_s = 48\text{ kHz}$ ,  $R_L = 8\ \Omega + 22\ \mu\text{H}$ , Analog Gain = 16.4dBV(SPK mode x3.0),  
 $T_A = +25\text{ }^\circ\text{C}$ , unless otherwise specified.

| Parameter                                  | Symbol               | Condition                                                                                               | Min.                  | Typ.                  | Max.                  | Unit             |
|--------------------------------------------|----------------------|---------------------------------------------------------------------------------------------------------|-----------------------|-----------------------|-----------------------|------------------|
| <b>Power Supplies</b>                      |                      |                                                                                                         |                       |                       |                       |                  |
| Shutdown Current at VBAT                   | $I_{SDBAT}$          | Software shutdown                                                                                       |                       | 5                     | 40                    | $\mu\text{A}$    |
| Shutdown Current at DVDD                   | $I_{SDVDD}$          | Software shutdown                                                                                       |                       | 4                     | 100                   | $\mu\text{A}$    |
| Reference Voltage at VREF                  | $V_{VREF}$           | Bias enable, no signal,<br>FLT_VDD_GAIN = 4'b1010<br>for 3.05 V                                         |                       | 3.05                  | 3.12                  | V                |
| Idle-mode Current at VBAT                  | $I_{IDBAT}$          | Audio enable, no signal                                                                                 |                       | 3.5                   | 7.5                   | mA               |
| Idle-mode Current at DVDD                  | $I_{IDVDD}$          | Audio enable, no signal                                                                                 |                       | 5.8                   | 8                     | mA               |
| <b>Boost Converter</b>                     |                      |                                                                                                         |                       |                       |                       |                  |
| Boost Output Voltage                       | $V_{BST}$            | $I_{LOAD} = 0\text{ mA}$                                                                                | 9.8                   | 10.0                  | 10.2                  | V                |
| Overvoltage Limit                          | $V_{OVBST}$          | $V_{BST}$ rising                                                                                        |                       | $V_{BST} \times 1.12$ |                       | V                |
| Undervoltage Protection                    | $V_{UVBST}$          | $V_{BAT}$ falling                                                                                       | 2.10                  | 2.45                  | 2.70                  | V                |
| Boost Switching Frequency                  | $F_{SWBST}$          | BST_OSC = 011                                                                                           | 1.95                  | 2.05                  | 2.15                  | MHz              |
| Boost Current Limit                        | $I_{LMBST}$          | SET_OCL = 010                                                                                           | 2.6                   | 3.0                   | 3.5                   | A                |
| Boost Overcurrent Protection <sup>1)</sup> | $I_{OCBST}$          | SET_OCL = 010                                                                                           |                       | 4.2                   |                       | A                |
| <b>Class-D Audio Amplifier</b>             |                      |                                                                                                         |                       |                       |                       |                  |
| Output Offset Voltage                      | $V_{OS}$             | Output muted, Receiver mode                                                                             | -0.8                  | 0                     | 0.8                   | mV               |
| Class-D Switching Frequency                | $F_{SWOUT}$          | FREQ_SEL = 0                                                                                            | 400                   | 470                   | 550                   | kHz              |
| Audio Overcurrent Protection <sup>1)</sup> | $I_{OCOUT}$          |                                                                                                         | 2.0                   |                       |                       | A                |
| Output Power                               | $P_O$                | $V_{BST} = 8.5\text{ V}$ , 1 kHz,<br>THD+N $\leq 1\%$ ,<br>$R_L = 8\ \Omega$ , $V_{BAT} = 4.4\text{ V}$ |                       | 4.0                   |                       | W                |
| THD+N                                      | THD+N                | 1 kHz, $P_O = 1\text{ W}$                                                                               |                       | 0.01                  |                       | %                |
| Noise <sup>1)</sup>                        | $V_{no}$             | A-weighted, no input signal,<br>Receiver mode                                                           |                       | 8.5                   |                       | $\mu\text{V}$    |
| Signal to Noise Ratio                      | SNR                  | $V_{BST} = 8.5\text{ V}$ , 1 kHz,<br>THD+N $\leq 1\%$ , A-weighted                                      |                       | 105                   |                       | dB               |
| PSRR at VBAT <sup>1)</sup>                 | PSRR <sub>BAT</sub>  | 217 Hz, $V_{RIPP} = 0.2\text{ V}_{PP}$                                                                  |                       | 80                    |                       | dB               |
|                                            |                      | 1 kHz, $V_{RIPP} = 0.2\text{ V}_{PP}$                                                                   |                       | 80                    |                       | dB               |
| PSRR at DVDD <sup>1)</sup>                 | PSRR <sub>DVDD</sub> | 217 Hz, $V_{RIPP} = 0.1\text{ V}_{PP}$                                                                  |                       | 90                    |                       | dB               |
|                                            |                      | 1 kHz, $V_{RIPP} = 0.1\text{ V}_{PP}$                                                                   |                       | 90                    |                       | dB               |
| Output Power Efficiency                    | $\eta_{po1}^{1)}$    | $P_O = 0.5\text{ W}$ , $V_{BAT} = 4.4\text{ V}$                                                         |                       | 90                    |                       | %                |
|                                            | $\eta_{po2}$         | $P_O = 2.0\text{ W}$ , $V_{BAT} = 4.4\text{ V}$                                                         |                       | 84                    |                       | %                |
| <b>Digital I/O</b>                         |                      |                                                                                                         |                       |                       |                       |                  |
| High Input Voltage                         | $V_{IH}$             |                                                                                                         | $V_{DVDD} \times 0.8$ |                       |                       | V                |
| Low Input Voltage                          | $V_{IL}$             |                                                                                                         |                       |                       | $V_{DVDD} \times 0.2$ | V                |
| High Input Leakage Current                 | $I_{LKH}$            | $V_{DVDD} = 1.95\text{ V}$ , $V_{IN} = 1.95\text{ V}$                                                   | -1                    |                       | 1                     | $\mu\text{A}$    |
| Low Input Leakage Current                  | $I_{LKL}$            | $V_{DVDD} = 1.95\text{ V}$ , $V_{IN} = 0\text{ V}$                                                      | -1                    |                       | 1                     | $\mu\text{A}$    |
| High Output Voltage                        | $V_{OH}$             |                                                                                                         | $V_{DVDD} \times 0.8$ |                       |                       | V                |
| Low Output Voltage                         | $V_{OL}$             |                                                                                                         |                       |                       | $V_{DVDD} \times 0.2$ | V                |
| <b>Thermal Protection</b>                  |                      |                                                                                                         |                       |                       |                       |                  |
| Temperature Shutdown                       | $T_{SD}$             |                                                                                                         |                       | 150                   |                       | $^\circ\text{C}$ |

**Note**

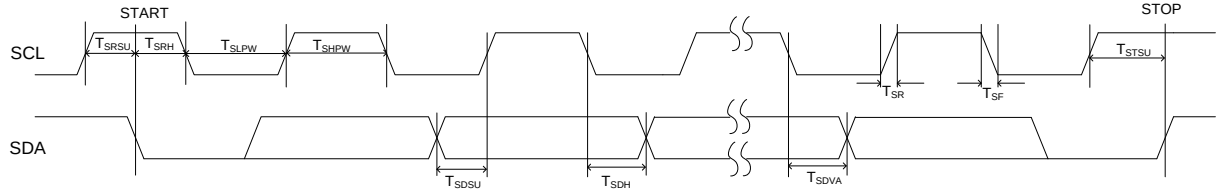
1) Specified by design

## Digital Audio Interface Timing for I<sup>2</sup>S



| Parameter             | Symbol     | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|------------|-----------|------|------|------|------|
| SCK Cycle Time        | $T_{SCY}$  |           | 80   |      |      | ns   |
| SCK High Pulse Width  | $T_{SCH}$  |           | 40   |      |      | ns   |
| SCK Low Pulse Width   | $T_{SCL}$  |           | 40   |      |      | ns   |
| LRCK Frequency        |            |           | 8    |      | 192  | kHz  |
| LRCK Setup Time       | $T_{LRSU}$ |           | 7    |      |      | ns   |
| LRCK Hold Time        | $T_{LRH}$  |           | 5    |      |      | ns   |
| SDI Setup Time        | $T_{DSU}$  |           | 7    |      |      | ns   |
| SDI Hold Time         | $T_{DH}$   |           | 5    |      |      | ns   |
| SDO Propagation Delay | $T_{DD}$   |           | 0    |      | 12   | ns   |

## Control Interface Timing for I<sup>2</sup>C



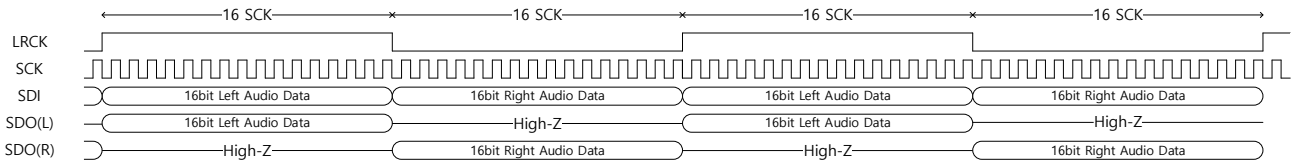
| Parameter                        | Symbol     | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|------------|-----------|------|------|------|------|
| SCL Frequency                    |            |           |      | 400  | 1000 | kHz  |
| SCL Low Pulse Width              | $T_{SLPW}$ |           | 500  |      |      | ns   |
| SCL High Pulse Width             | $T_{SHPW}$ |           | 260  |      |      | ns   |
| Hold Time at START               | $T_{SRH}$  |           | 260  |      |      | ns   |
| Setup Time at START              | $T_{SRSU}$ |           | 260  |      |      | ns   |
| SDA, SCL Rising Time             | $T_{SR}$   |           |      |      | 120  | ns   |
| SDA, SCL Falling Time            | $T_{SF}$   |           |      |      | 120  | ns   |
| Setup Time at STOP               | $T_{STSU}$ |           | 260  |      |      | ns   |
| SDA Setup Time                   | $T_{SDSU}$ |           | 50   |      |      | ns   |
| SDA Hold Time                    | $T_{SDH}$  |           | 0    |      |      | ns   |
| SDA Valid Time (acknowledge)     | $T_{SDVA}$ |           |      |      | 450  | ns   |
| Pulse Width of Spikes Suppressed | $T_{SPW}$  |           | 0    |      | 20   | ns   |

## Condition for Selecting I<sup>2</sup>C Addresses

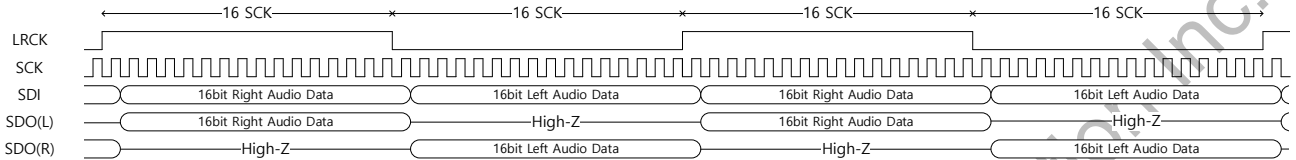
| Parameter                                   | Symbol     | Condition | Min. | Typ. | Max. | Unit |
|---------------------------------------------|------------|-----------|------|------|------|------|
| I <sup>2</sup> C Address Selection Resistor | $R_{ADDR}$ |           | 20   | 22   | 24   | kΩ   |

## Interface Format for Audio Interface

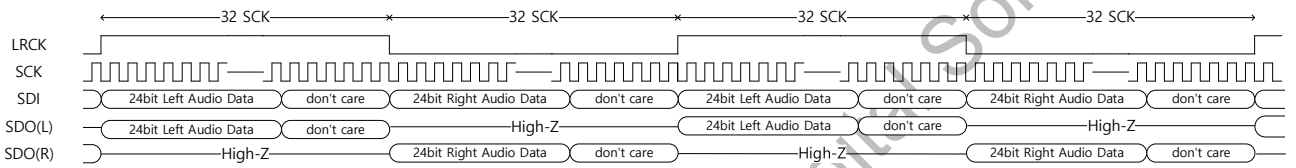
### LJ 32 fs



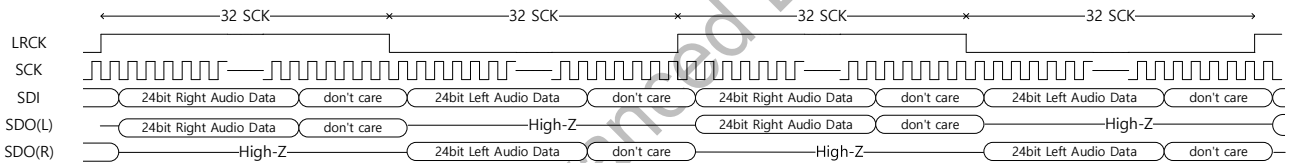
### I<sup>2</sup>S 32 fs



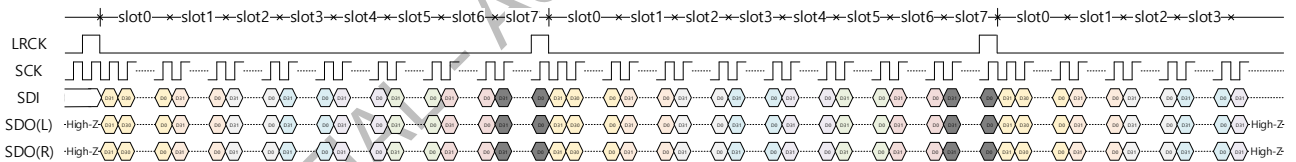
### LJ 64 fs



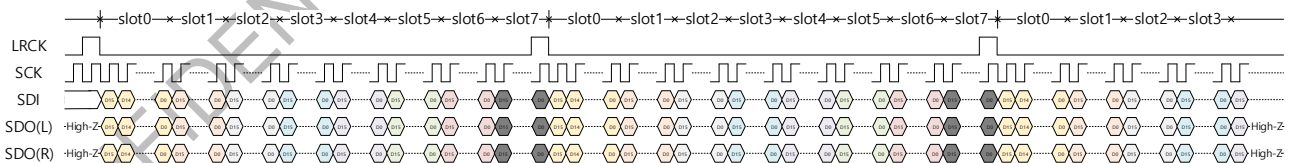
### I<sup>2</sup>S 64 fs



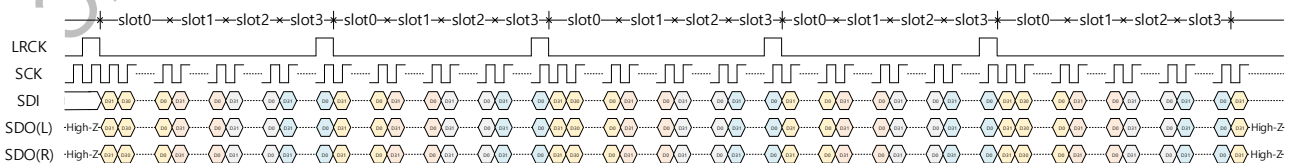
### TDM 8-CH (slot), fs = 48 kHz, data = 32-bit



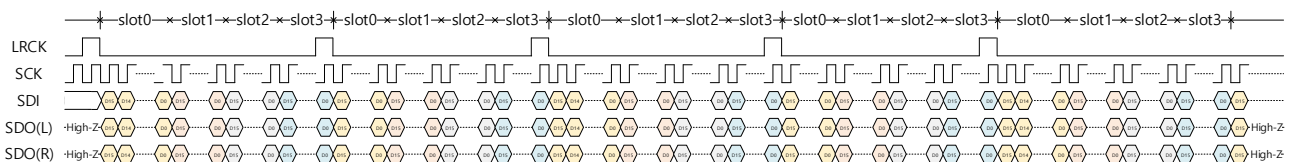
### TDM 8-CH (slot), fs = 48 kHz, data = 16-bit



### TDM 4-CH (slot), fs = 48 kHz, data = 32-bit



### TDM 4-CH (slot), fs = 48 kHz, data = 16-bit



## Device Functional Description

### Digital Signal Processing

#### High Pass Filters

There is a 1<sup>st</sup> order high pass filter in the DSP input. The frequency range is from 0 Hz (off) to 1 kHz and can be controlled by the FOA coefficient of the bass boost. The registers are 0x15[7:0] and 0x19[6:5].

#### Left / Right Input Mixer

Left and right input signals can be mixed with different gain levels.

#### Multi-Channel TDM Mode

SMA1857 supports four TDM modes with 4-CH / 16-bit, 4-CH / 32-bit, 8-CH / 16-bit and 8-CH / 32-bit of short sync TDM format ( $f_s = 48$  kHz).

### Stereo Mode Connection

If using two chips for stereo, the I<sup>2</sup>S line can be shared, and one chip would be set to the left out and the other to the right out.

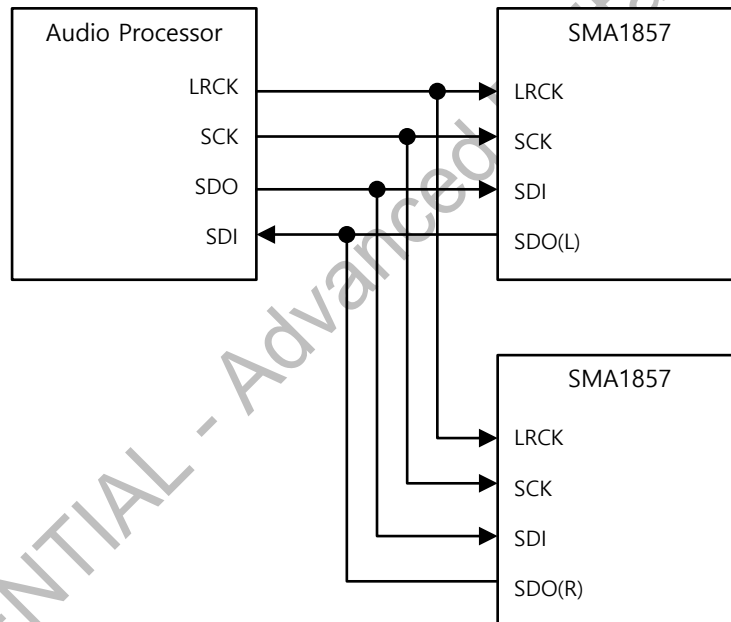


Figure 1. Stereo Mode Connection

\*SDO pin needs a pull-down resistor when the audio processor SDI input is high impedance.

A register for SDO pin should be considered when two SMA1857 chips are used to configure stereo application. Based on I<sup>2</sup>S mode, both of two SMA1857 chips must carry data on each channel for left or right. The SDO pin of one chip must be set to High-Z when the SDO pin of the other chip is carrying data. Please refer to the 0xA2[1] register as below.

Table 1. Register Setting for SDO pin

| Register and Name     | Left Channel        | Right Channel       |
|-----------------------|---------------------|---------------------|
| 0xA2[1] SDO_PAD_CTRL1 | 0: High-Z at LRCK H | 1: High-Z at LRCK L |

### Output Data Selection

The SMA1857 has one channel output. The output data is determined by the register setting, and it can be the left, right, or mixed data of stereo input.

## Gain Stages

The SMA1857's output level can be calculated based on the digital input signal level and selected gain according to the following equation:

$$\text{Output Signal Gain [dB]} = \text{Digital Gain [dB]} + \text{Digital Fine Gain [dB]} + \text{Analog Gain [dB]}$$

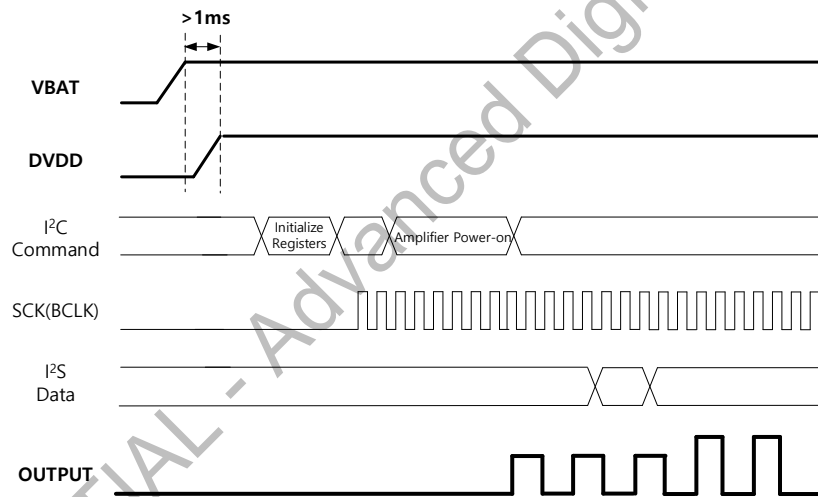
Ex.) Digital Gain -1dB, Digital Fine Gain 0dB, Analog Gain 16.4dB → Output Signal Gain 15.4 dB → Output Level 5.89Vrms

**Table 2. Gain Stages and Ranges**

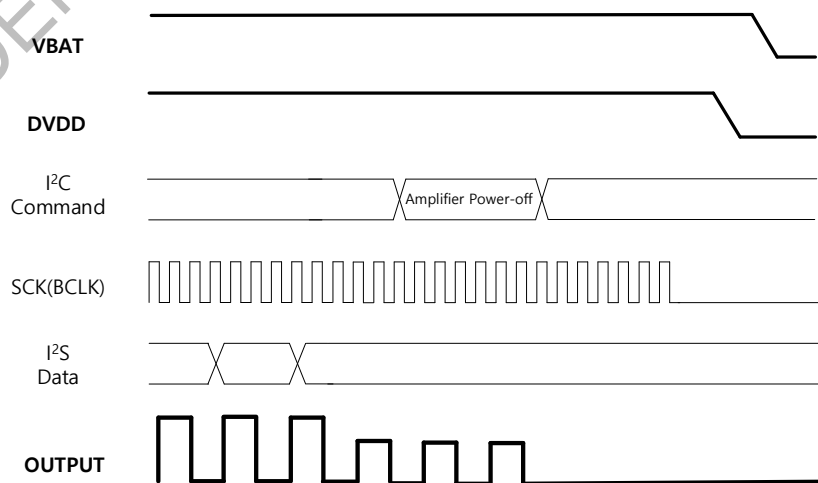
| Gain Stages                 | Tunable Range                                           | Gain Step | Note                                   |
|-----------------------------|---------------------------------------------------------|-----------|----------------------------------------|
| Digital Gain                | +24 dB ~ -65 dB, -inf.                                  | 0.5 dB    | Soft step                              |
| Digital Gain (fine gain)    | -3.0 dB ~ 3.0 dB                                        | 0.125 dB  | Hard step                              |
| D/A Conversion Gain (fixed) | 1 [Vrms / 0dBFS]                                        | -         | Fine tuning by I2C                     |
| Analog Gain                 | 1.1, 2.4, 6.6, 7.9 [V/V]<br>(0.8, 7.6, 16.4, 17.9 [dB]) |           | D/A output to<br>Amplifier output gain |

## Power Sequence

The SMA1857 needs VBAT (battery) and DVDD. SCK of I<sup>2</sup>S is the input clock of PLL for the system clock in a typical application. In this case, turning SCK off during output operation is not allowed.



**Figure 2. Power-on Sequence**



**Figure 3. Power-off Sequence**

## Application Information

### Typical Application Circuit

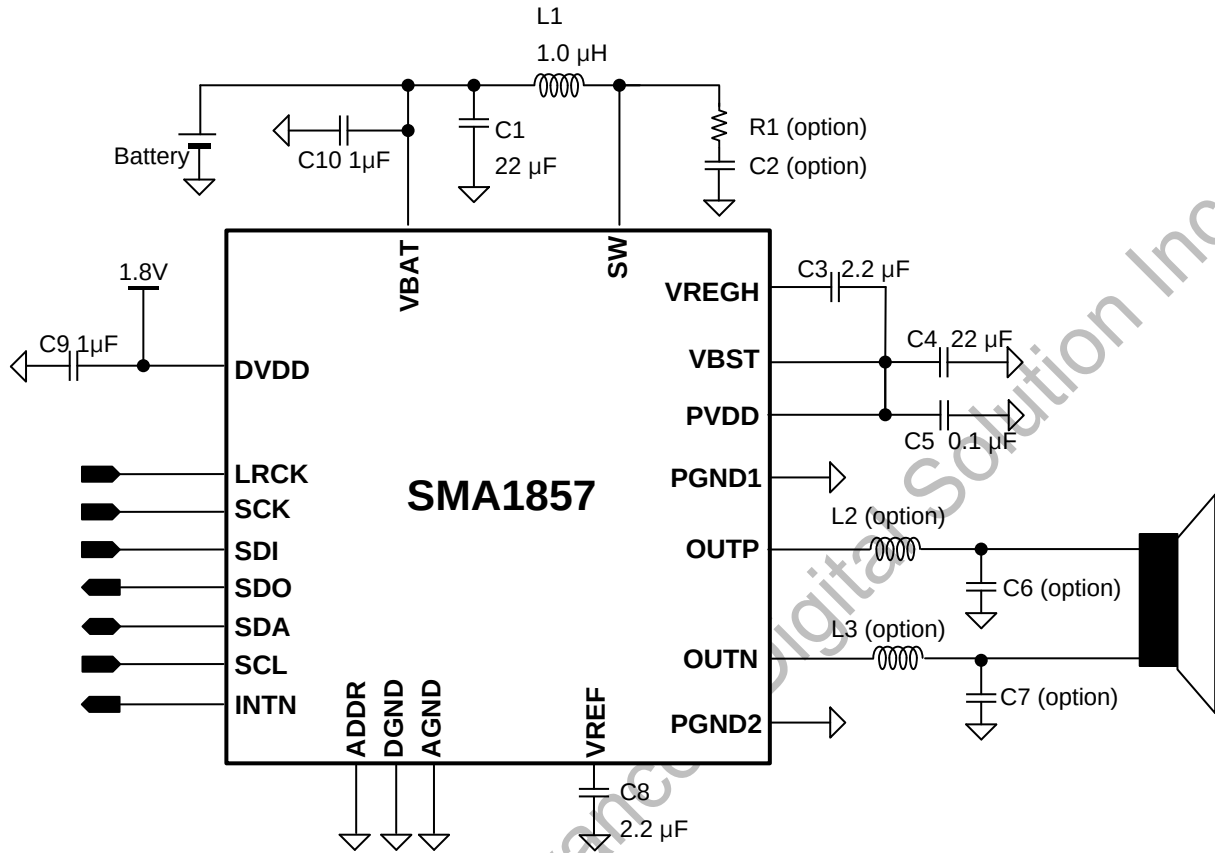


Figure 4. Typical Application Circuit

Table 3. Recommended Components

| Components | Description                         | Specification                                                                                                                                              |
|------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| L1         | Inductor for Boost Converter        | 1.0 $\mu$ H, current rate > 4.0 A                                                                                                                          |
| C1         | Boost Converter Input Capacitor.    | The typical value is 22 $\mu$ F if battery is connected. If there is no battery at boost converter input, the total capacitance should be over 60 $\mu$ F. |
| C4         | Boost Converter Output Capacitor    | Capacitance is 22 $\mu$ F to 33 $\mu$ F and close to VBST. The minimum capacitance at 10 V derating is 3 $\mu$ F.                                          |
| R1, C2     | Snubber Filter on the SW (optional) | It depends on the PCB condition. The typical value is 4.7 $\Omega$ and 1 nF if it is needed.                                                               |
| L2, L3     | EMI Filter Inductors (optional)     | Bead, 120 $\Omega$ at 100 MHz, current rate > 1.2 A                                                                                                        |
| C6, C7     | EMI Filter Capacitors (optional)    | Must use L2 and L3 if C6 and C7 are used. The maximum value C6 and C7 are 1 nF.                                                                            |

### EMI Filter on Speaker Output

To reduce EMI from speaker output PWM, a Bead-C filter on speaker output as shown in Figure 5 is needed. It is not allowed to use of only the capacitor on speaker output without the Bead. C6 and C7 must be placed after the bead. Also, the capacitance of C6 and C7 should be under 1 nF.

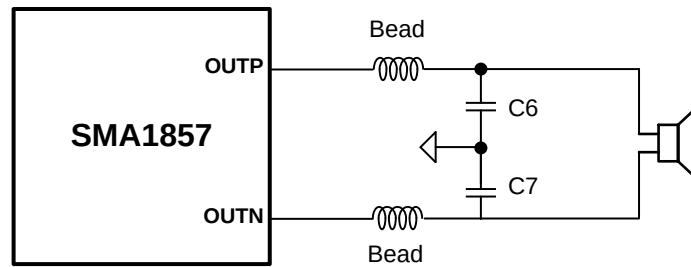


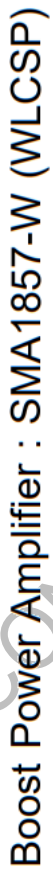
Figure 5. Bead-C Filter

### Multiple I<sup>2</sup>C Address

The SMA1857 operates as an I<sup>2</sup>C slave over the DVDD voltage range. It is adjustable to one of four I<sup>2</sup>C addresses. This allows multiple SMA1857 devices in a system to connect to the same I<sup>2</sup>C bus. The I<sup>2</sup>C address can be set by using the ADDR pin connection in Table 4.

Table 4. I<sup>2</sup>C Address Selection

| ADDR Pin Connection                    | I <sup>2</sup> C Slave Device Address |
|----------------------------------------|---------------------------------------|
| Short to DGND                          | 0x1E                                  |
| Connection to DGND using 22 k $\Omega$ | 0x3E                                  |
| Connection to DVDD using 22 k $\Omega$ | 0x5E                                  |
| Short to DVDD                          | 0x7E                                  |



**Figure 6. Reference Schematic for WLCS Package**

**BST SW / SPK Out Off Slope Control**

| Register | Function | Name          | Bit |   |   |   |   |   |   |   | Description                                                            |
|----------|----------|---------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------|
|          |          |               | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                        |
| 0x0B     | BST_TEST | EN_STP        |     |   |   |   |   |   |   |   | Shoot-Through Protection<br>0: Disable<br>1: Enable                    |
|          |          | DIS_SHORT_P   |     |   |   |   |   |   |   |   | Short Protection of BST<br>0: Enable<br>1: Disable                     |
|          |          | OCP_TEST      |     |   |   |   |   |   |   |   | OCP Test Mode<br>0: Normal mode<br>1: OCP test mode                    |
|          |          | BST_FAST_LEBN |     |   |   |   |   |   |   |   | Leading Edge Blanking<br>0: Short LEB<br>1: Long LEB                   |
|          |          | OCL_TEST      |     |   |   |   |   |   |   |   | OCL Test Mode<br>0: Normal mode<br>1: OCL test mode                    |
|          |          | VCOMP         |     |   |   |   |   |   |   |   | VCOMP Monitoring<br>0: Normal mode<br>1: VCOMP voltage monitoring mode |
|          |          | PMOS_ON       |     |   |   |   |   |   |   |   | PMOS Test Mode<br>0: Normal mode<br>1: PMOS test mode – PMOS on        |
|          |          | NMOS_ON       |     |   |   |   |   |   |   |   | NMOS Test Mode<br>0: Normal mode<br>1: NMOS test mode – NMOS on        |
|          |          | Default       | 1   | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0x90                                                                   |

| Register | Function       | Name      | Bit |   |   |   |   |   |   |   | Description                                                                 |
|----------|----------------|-----------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------|
|          |                |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                             |
| 0x0C     | Boost Control8 | SET_OCP_H |     |   |   |   |   |   |   |   | Control High Side OCP Level<br>00: 4.5      01: 3.2<br>10: 2.1      11: 0.9 |
|          |                | -         |     |   |   |   |   |   |   |   | Reserved                                                                    |
|          |                | LOW_OCLN  |     |   |   |   |   |   |   |   | Set Low OCL mode<br>0: Low OCL mode<br>1: Normal mode                       |
|          |                | -         |     |   |   |   |   |   |   |   | Reserved                                                                    |
|          |                | Default   | 1   | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0x8C                                                                        |

| Register | Function | Name     | Bit |   |   |   |   |   |   |   | Description                                                                           |
|----------|----------|----------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------|
|          |          |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                       |
| 0x0D     | SPK_TEST | -        |     |   |   |   |   |   |   |   | Reserved                                                                              |
|          |          | TSD_TEST |     |   |   |   |   |   |   |   | Enable TSD Monitoring at FLTVDD<br>0: Normal mode<br>1: TSD Test mode                 |
|          |          | VREF_MON |     |   |   |   |   |   |   |   | Enable VREF Monitoring at FLTVDD<br>0: Normal mode<br>1: VREF voltage monitoring mode |
|          |          | -        |     |   |   |   |   |   |   |   | Reserved                                                                              |
|          |          | Default  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                  |

## PCB Layout Example

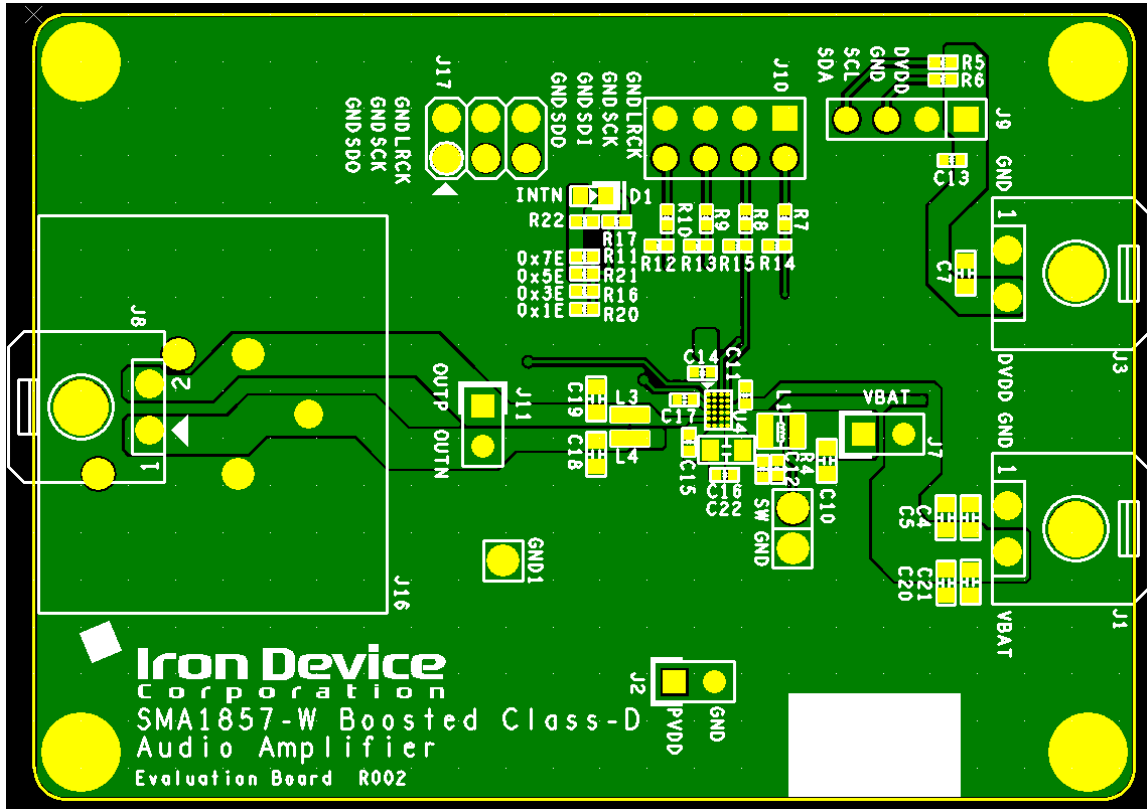


Figure 7. Layout Example - Layer TOP

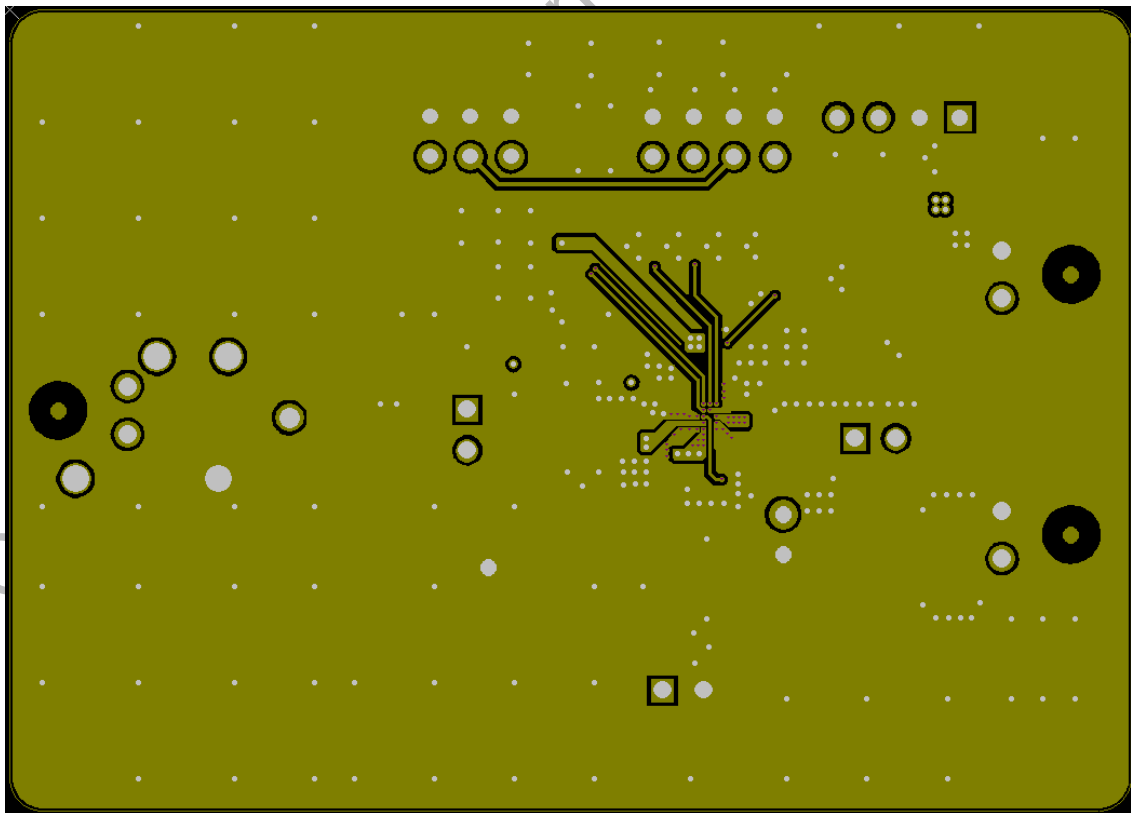


Figure 8. Layout Example - Layer 2

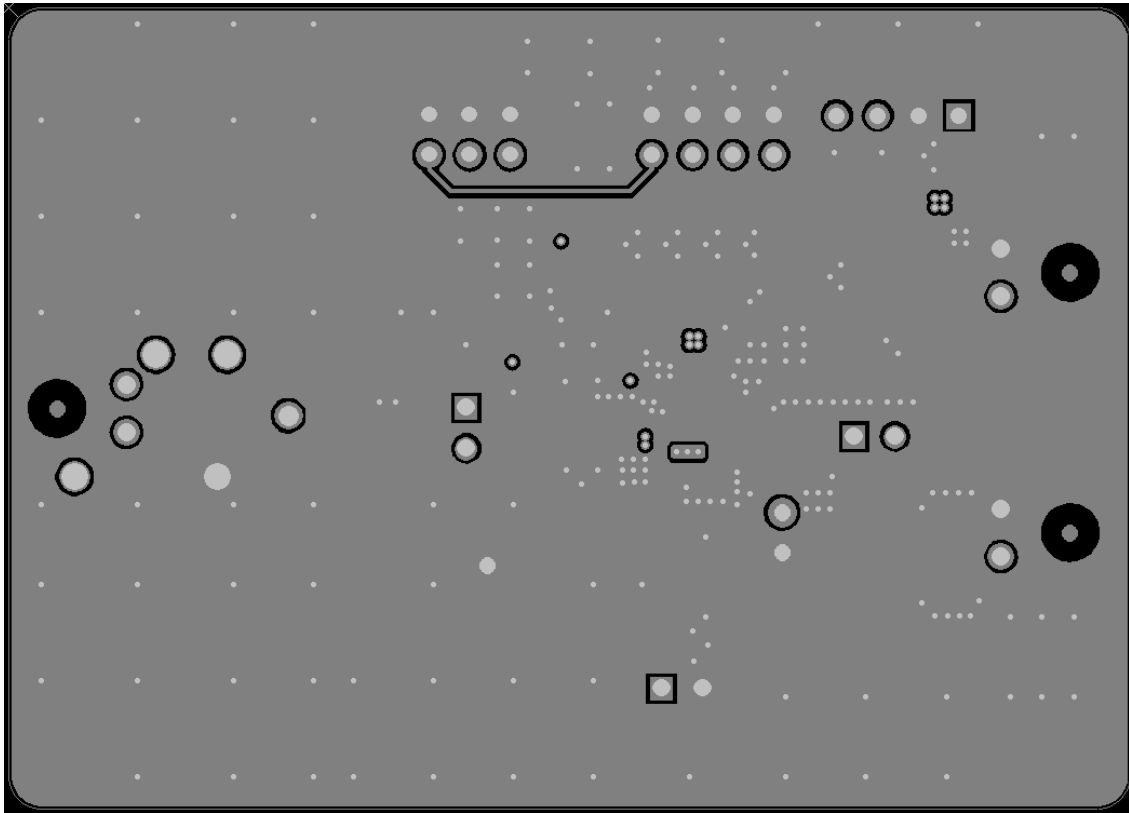


Figure 9. Layout Example - Layer 3

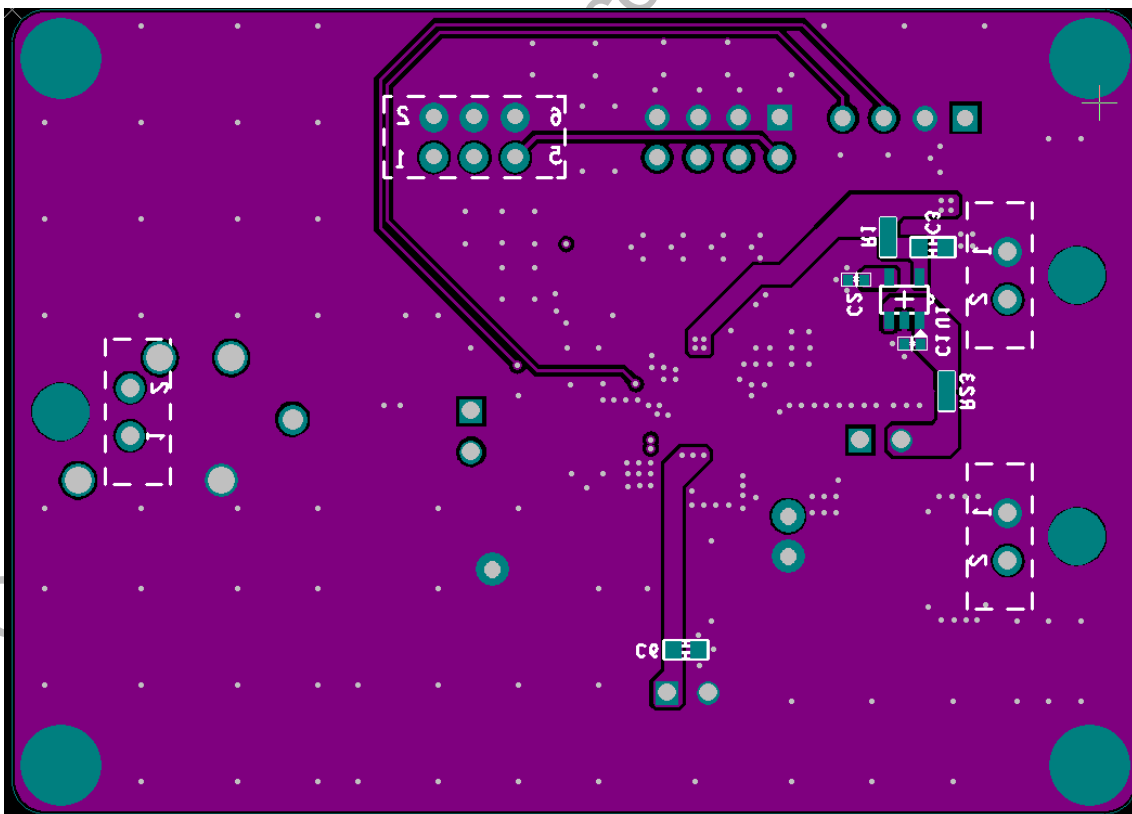


Figure 10. Layout Example - Layer BOTTOM

## PCB Layout Considerations

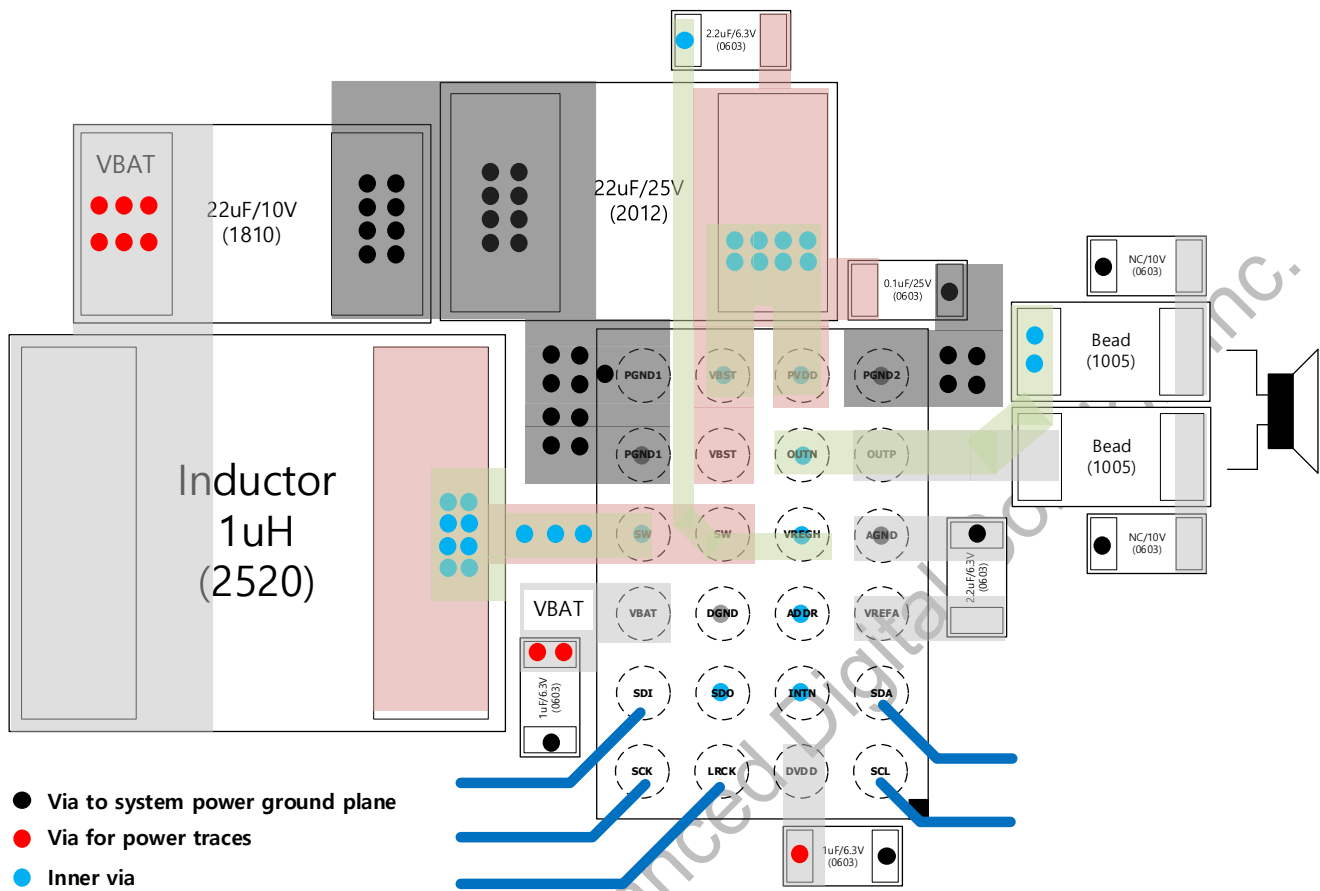


Figure 11. PCB Artwork Recommendation

## Best Practice

A small guide on how to trace the connection for SMA1857.

- Sensible traces must be drawn far away from aggressive traces.
- The short and wide trace of the PGND pin must be drawn to the POWER GND of PCB on the same layer for above the maximum 4 A current drive. It is helpful to add another trace on the inner layer with an inner via from the PGND pin to POWER GND to reduce the ground trace's impedance (inductance and resistance).
- Booster input line from a battery to the SW pin through a boost inductor should be traced above the maximum 4 A current drive. It must be separated from the PMIC for the application processors because the PMIC can create audible noise.
- The trace of the VBAT pin must be drawn far away from the booster input line with a bead and a capacitor to be used as a stable internal reference without ripple and noise.
- The booster inductor should be as near as possible to the IC.
- Output signals (OUTP and OUTN) should be traced above the 1.2 A current drive up to the audio connector.
- Minimize the impedance between the PGND ball and the ground plane.

## Traces' Sensibility

| Type                | Signal Example                     |
|---------------------|------------------------------------|
| Sensible            | SW, VBST, PVDD, OUTP, OUTN         |
| Moderately sensible | VBAT                               |
| Aggressor           | I <sup>2</sup> C, I <sup>2</sup> S |
| Normal              | Other signals                      |

**I<sup>2</sup>C Control Registers****Slave Address (four I<sup>2</sup>C addresses)**

[ADDR] = Short to DGND

The device supports 7-bit addressing only (address: 0x1E).

| Bit 7, MSB | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0, LSB |
|------------|-------|-------|-------|-------|-------|-------|------------|
| 0          | 0     | 1     | 1     | 1     | 1     | 0     | R/W        |

Registers are R/W (read / write) except those specified as 'Read-Only'

[ADDR] = Connection to DGND using 22 kΩ

The device supports 7-bit addressing only (address: 0x3E).

| Bit 7, MSB | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0, LSB |
|------------|-------|-------|-------|-------|-------|-------|------------|
| 0          | 1     | 1     | 1     | 1     | 1     | 0     | R/W        |

Registers are R/W (read / write) except those specified as 'Read-Only'

[ADDR] = Connection to DVDD using 22 kΩ

The device supports 7-bit addressing only (address: 0x5E).

| Bit 7, MSB | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0, LSB |
|------------|-------|-------|-------|-------|-------|-------|------------|
| 1          | 0     | 1     | 1     | 1     | 1     | 0     | R/W        |

Registers are R/W (read / write) except those specified as 'Read-Only'

[ADDR] = Short to DVDD

The device supports 7-bit addressing only (address: 0x7E).

| Bit 7, MSB | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0, LSB |
|------------|-------|-------|-------|-------|-------|-------|------------|
| 1          | 1     | 1     | 1     | 1     | 1     | 0     | R/W        |

Registers are R/W (read / write) except those specified as 'Read-Only'

## Device Register Map

| Adress | Function             | 7            | 6             | 5                 | 4             | 3          | 2            | 1             | 0        | Default |      |
|--------|----------------------|--------------|---------------|-------------------|---------------|------------|--------------|---------------|----------|---------|------|
| 0x00   | SystemCTRL           | Reserved     |               |                   |               |            |              | RESETBYI2C    | POWERUP  | 0X80    |      |
| 0x01   | InputCTRL1           | Reserved     | I2SMODE       |                   |               | LEFTPOL    | SCK_RISING   | Reserved      |          | 0X00    |      |
| 0x02   | BrownOutProtection1  | BO_LVL1      |               |                   |               |            |              |               |          |         | 0X6D |
| 0x03   | BrownOutProtection2  | BO_LVL2      |               |                   |               |            |              |               |          |         | 0X67 |
| 0x04   | BrownOutProtection3  | BO_LVL3      |               |                   |               |            |              |               |          |         | 0X63 |
| 0x05   | BrownOutProtection8  | BO_LVL4      |               |                   |               |            |              |               |          |         | 0X5A |
| 0x06   | BrownOutProtection9  | BO_LVL5      |               |                   |               |            |              |               |          |         | 0X54 |
| 0x07   | BrownOutProtection10 | BO_LVL6      |               |                   |               |            |              |               |          |         | 0X4D |
| 0x08   | BrownOutProtection11 | BO_LVL7      |               |                   |               |            |              |               |          |         | 0X4B |
| 0x09   | OutputCTRL           | PORT_CONFIG  |               | SDO_OUT1_SEL      |               |            | SDO_OUT0_SEL |               |          | 0X00    |      |
| 0x0A   | SPK_VOL              | SPKVOL       |               |                   |               |            |              |               |          |         | 0X58 |
| 0x0B   | BST_TEST             | EN_STP       | DIS_SHORT_P   | OCP_TEST          | BST_FAST_LEBN | OCL_TEST   | VCOMP        | PMOS_ON       | NMOS_ON  | 0X90    |      |
| 0x0C   | BoostControl8        | SET_OCP_H    |               | Reserved          |               | LOW_OCLN   | Reserved     |               |          | 0X8C    |      |
| 0x0D   | SPK_TEST             | Reserved     |               |                   | TSD_TEST      | VREF_MON   | Reserved     |               |          | 0X00    |      |
| 0x0E   | MUTE_VOL_CTRL        | VOL_SLOPE    |               | MUTE_SLOPE        |               | Reserved   |              |               | SPK_MUTE | 0XAF    |      |
| 0x0F   | VBAT_TEMP_SENSING    | SENSING_PD   | VBAT_LPF_BYP  |                   | Reserved      |            |              | CLK_FREQUENCY |          | 0XE0    |      |
| 0x10   | SystemCTRL1          | Reserved     |               |                   | SPKMODE       |            |              | Reserved      |          | 0X00    |      |
| 0x11   | SystemCTRL2          | Reserved     | SPKSET        |                   | LR_DATA_SW    | Reserved   |              |               | MONO_MIX | 0X00    |      |
| 0x12   | SystemCTRL3          | INPUT        |               | INPUT_R           |               | Reserved   |              |               |          | 0X00    |      |
| 0x13   | DELAY                | Reserved     |               |                   | BYP_DLY       | SET_DLY    |              |               |          | 0X09    |      |
| 0x14   | Modulator            | SPK_HYSFB    |               | SPK_BDELAY        |               |            |              |               |          | 0X60    |      |
| 0x15   | BassSpk1             | SBSPK_F0A_M  |               |                   |               |            |              |               |          |         | 0X01 |
| 0x16   | BassSpk2             | SBSPK_F0B1_M |               |                   |               |            |              |               |          |         | 0X0F |
| 0x17   | BassSpk3             | SBSPK_F0B2_M |               |                   |               |            |              |               |          |         | 0X0F |
| 0x18   | BassSpk4             | SBSPK_F0C_M  |               |                   |               |            |              |               |          |         | 0X0F |
| 0x19   | BassSpk5             | Reserved     | SBSPK_LSB1    |                   |               |            |              | SBSPKGAIN     |          | 0X00    |      |
| 0x1A   | BassSpk6             | Reserved     | SBSPK_LSB2    |                   |               |            |              | SBSPKTHRES    |          | 0X00    |      |
| 0x1B   | BassSpk7             | Reserved     |               |                   |               | SBSPKTIME  |              | SBSPKFB_TYPE  | SBSPKSEL | 0X00    |      |
| 0x1C   | BrownOutProtection20 | Reserved     |               |                   |               | HOLD_TIME  |              |               |          | 0X00    |      |
| 0x1D   | BrownOutProtection0  | BOP_PDN      | Reserved      |                   |               | BO_HYS     |              |               |          | 0X08    |      |
| 0x1E   | TONE_GENERATOR       | Reserved     | BYP_TONE_FINE | TONE_AUDIO_MIX_ON | TONE_FREQ     |            |              |               | TONE_ON  | 0XA1    |      |
| 0x1F   | TONE/FINEVOLUME      | FINE_VOL     |               |                   |               |            | TONE_VOL     |               |          | 0X67    |      |
| 0x20   | Reserved             | Reserved     |               |                   |               |            |              |               |          |         | 0X00 |
| 0x21   | Reserved             | Reserved     |               |                   |               |            |              |               |          |         | 0XAA |
| 0x22   | COMP_HYSSelector     | Reserved     |               |                   |               |            | COMP_HYS_SEL |               |          | 0X00    |      |
| 0x23   | CompLim1             | SPK_RATIO    | SPK_HRDLIMIT  |                   | SPK_LIMTHR    |            |              |               |          | 0X1F    |      |
| 0x24   | CompLim2             | SPK_LIMATT   |               |                   |               | SPK_LIMREL |              |               |          | 0X00    |      |
| 0x25   | CompLim3             | SPK_COMATT   |               |                   |               | SPK_COMREL |              |               |          | 0X00    |      |
| 0x26   | CompLim4             | SPK_COMTHRES |               |                   |               |            |              |               |          |         | 0X04 |
| 0x27   | BrownOutProtection4  | BOP_LVL1     |               |                   | LIM_THR1      |            |              |               |          | 0X1C    |      |
| 0x28   | BrownOutProtection5  | BOP_LVL2     |               |                   | LIM_THR2      |            |              |               |          | 0X1B    |      |
| 0x29   | BrownOutProtection12 | BOP_LVL3     |               |                   | LIM_THR3      |            |              |               |          | 0X18    |      |

| Adress | Function                | 7            | 6           | 5            | 4                    | 3            | 2        | 1          | 0              | Default |
|--------|-------------------------|--------------|-------------|--------------|----------------------|--------------|----------|------------|----------------|---------|
| 0x2A   | BrownOutProtection13    | BOP_LVL4     |             |              | LIM_THR4             |              |          |            |                | 0X76    |
| 0x2B   | BrownOutProtection14    | BOP_LVL5     |             |              | LIM_THR5             |              |          |            |                | 0X94    |
| 0x2C   | BrownOutProtection15    | BOP_LVL6     |             |              | LIM_THR6             |              |          |            |                | 0XB3    |
| 0x2D   | BrownOutProtection6     | COMP_THRES1  |             |              |                      |              |          |            |                | 0XE6    |
| 0x2E   | BrownOutProtection7     | COMP_THRES2  |             |              |                      |              |          |            |                | 0XD9    |
| 0x2F   | BrownOutProtection16    | COMP_THRES3  |             |              |                      |              |          |            |                | 0XC0    |
| 0x30   | BrownOutProtection17    | COMP_THRES4  |             |              |                      |              |          |            |                | 0XB3    |
| 0x31   | BrownOutProtection18    | COMP_THRES5  |             |              |                      |              |          |            |                | 0XA6    |
| 0x32   | BrownOutProtection19    | COMP_THRES6  |             |              |                      |              |          |            |                | 0X99    |
| 0x33   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X00    |
| 0x34   | OCP_SPK                 | Reserved     |             |              |                      | OCP_FILTER   |          | OCP_LVL_N  |                | 0X09    |
| 0x35   | FDPECControl0           | I_OP1        |             | I_OP2        |                      | AMP_RES      | SYNC_RES | FDPEC_GAIN |                | 0X56    |
| 0x36   | Protection              | EGDE_DIS     | LR_DELAY    |              | TEST_OCP_STEREO_MODE | SPK_OCP_DIS  | OCP_MODE | OTP_MODE   |                | 0X92    |
| 0x37   | SlopeCTRL               | Reserved     |             | SPK_SLOPE    |                      | SPK_DEADTIME |          |            |                | 0X25    |
| 0x38   | PowerMeter              | PMT_EN       | PMT_INI     | PMT_ATK      |                      | PMT_REL      |          | NZ_VAL_1   |                | 0X31    |
| 0x39   | PMT_NZ_VAL              | NZ_VAL_2     |             |              |                      |              |          |            |                | 0X00    |
| 0x3A   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X00    |
| 0x3B   | Test1                   | CODE         |             |              |                      |              |          |            |                | 0X00    |
| 0x3C   | Test2                   | DIS_BSIDE    | SDM_DC      | SDM_SYNC_DIS | SPK_HSDM_BP          | SPK_OFF      | Reserved |            |                | 0X00    |
| 0x3D   | Test3                   | PWM_TIE_EN   | PWM_TIE_SEL | Reserved     |                      | SPK_5050     | Reserved | DC_CAL_DIS | NG_DIR_CTRL_EN | 0X00    |
| 0x3E   | DIG_IDLECURRENT_CONTROL | Reserved     | IDLE_TDM    | IDLE_SYNC    | IDLE_SOUT            | IDLE_RMS2    | IDLE_ENV | IDLE_BOP   | IDLE_PLLTEST   | 0X09    |
| 0x3F   | ATEST2                  | VREF_TEST    | TSD_ADJ     |              | AMP_RES_MODE         | LOW_PWR      | FREQ_SEL | SPK_DELAY  | SPK_FAST_OFF   | 0X0A    |
| 0x8B   | PLL_POST_N              | POST_N       |             |              |                      |              |          |            |                | 0X07    |
| 0x8C   | PLL_N                   | PLL_N        |             |              |                      |              |          |            |                | 0XE0    |
| 0x8D   | PLL_A_Setting           | VCO_AMP_CTRL |             | CP_AMP_CTRL  |                      | VCO_CTRL     |          |            |                | 0X8B    |
| 0x8E   | PLL_P,CP                | LF_3RD_EN    | LF_CTRL     | PFD_SEL      |                      | PLL_P        |          | CP_CTRL    |                | 0X10    |
| 0x8F   | ANA_TEST                | Reserved     |             |              | BST_OCP_CLR          | DIS_PVSS_SP  | LOW_UVLO | GM_CTRL    |                | 0X00    |
| 0x90   | CrestLim1               | CRSETLIM_1   |             |              |                      |              |          |            |                | 0X02    |
| 0x91   | CrestLim2               | CRSETLIM_2   |             |              |                      |              |          |            |                | 0X82    |
| 0x92   | FDPECControl1           | FLT_VDD_GAIN |             |              |                      | Reserved     | DIS_FCHG | Reserved   |                | 0XB0    |
| 0x93   | INTControl              | Reserved     |             |              |                      |              | SEL_INT  | CLR_INT    | DIS_INT        | 0X00    |
| 0x94   | BoostControl9           | SLOPE_OFF    |             | SLOPE        |                      | Reserved     | SET_RMP  |            |                | 0X54    |
| 0x95   | BoostControl10          | HIGH_PGAIN   | SET_OCL     |              |                      | SET_COMP     |          |            |                | 0XA4    |
| 0x96   | BoostControl11          | SET_DT       |             |              |                      | SET_DT_OFF   |          |            |                | 0X44    |
| 0x97   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X64    |
| 0x98   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X88    |
| 0x99   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X00    |
| 0x9A   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X00    |
| 0x9B   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X64    |
| 0x9C   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0XA4    |
| 0x9D   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X00    |
| 0x9E   | Reserved                | Reserved     |             |              |                      |              |          |            |                | 0X00    |

| Address | Function       | 7                | 6              | 5                 | 4                | 3            | 2                | 1             | 0               | Default |
|---------|----------------|------------------|----------------|-------------------|------------------|--------------|------------------|---------------|-----------------|---------|
| 0x9F    | Reserved       | Reserved         |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xA0    | PAD_CTRL0      | CLK_MON_SOURCE   |                | Reserved          |                  | AUDIO_PD     | SDO_PU           | INTN_PU       | I2C_PU          | 0X00    |
| 0xA1    | PAD_CTRL1      | INTN_DS          | SDO_DS         | SDA_DS            | LRCK_IE          | SCK_IE       | SDI_IE           | Reserved      |                 | 0X3F    |
| 0xA2    | TOP_MAN1       | Reserved         | PLL_PD         | PLL_DIV           |                  | N_TEST_HTOL  | LRSYNC_DIS       | SDO_IO        | SDO_OUTPUT2     | 0X4C    |
| 0xA3    | TOP_MAN2       | MON_OSC_PLL      |                | Reserved          |                  | SDO_OUPUT1   | SDO_OUTPUT3      | CLOCK_MON     | OSC_PD          | 0X28    |
| 0xA4    | TOP_MAN3       | INTERFACE        |                |                   | SCK_RATE         |              | DATA_W           |               | LRCK_POL        | 0X40    |
| 0xA5    | TDM1           | Reserved         | TDM_STEREO     | TDM_SLOT1_POS_RX  |                  |              | TDM_SLOT2_POS_RX |               |                 | 0X01    |
| 0xA6    | TDM2           | TDM_DL           | TDM_N_SLOT     | TDM_SLOT_POS_TX   |                  |              | TDM_SLOT2_POS_TX |               |                 | 0X41    |
| 0xA7    | CLK_MON        | CLK_MON_TIME_SEL |                | DITHER            | EN_A_TV          | TEST_LIMITER | Reserved         |               |                 | 0X00    |
| 0xA8    | BoostControl1  | Reserved         |                |                   | MIN_V            |              |                  |               |                 | 0X0C    |
| 0xA9    | BoostControl2  | SOFT_CLK         |                |                   | HEAD_ROOM        |              |                  |               |                 | 0X24    |
| 0xAA    | BoostControl3  | Reserved         |                | HOLD_TIME         |                  |              |                  |               |                 | 0X10    |
| 0xAB    | BoostControl4  | Reserved         |                |                   | BOOST_MAX        |              |                  |               |                 | 0X13    |
| 0xAC    | BoostControl5  | Reserved         | BOOST_MODE     |                   | SKIP_PULSE       |              |                  |               |                 | 0X10    |
| 0xAD    | BoostControl6  | RELEASE_TIME     |                |                   |                  |              |                  |               |                 | 0X10    |
| 0xAE    | BoostControl7  | BST_ON_DELAY     |                |                   | BST_FREQ         |              |                  | MIN_DUTY      |                 | 0XCD    |
| 0xAF    | LPF            | COEF_A           |                | COEF_B            |                  |              | COEF_C           |               |                 | 0X41    |
| 0xB0    | RMS_TC1        | PEAK_THR         | DATA_FORMAT    | Reserved          |                  |              | RMS_TIME_CONST   |               |                 | 0X07    |
| 0xB1    | RMS_TC2        | RMS_TIME_CONST2  |                |                   |                  |              |                  |               |                 | 0XFF    |
| 0xB2    | AVG_TC1        | Reserved         |                |                   |                  |              | AVG_TIME_CONST1  |               |                 | 0X07    |
| 0xB3    | AVG_TC2        | AVG_TIME_CONST2  |                |                   |                  |              |                  |               |                 | 0XFF    |
| 0xB4    | PR_VALUE1      | PR_VALUE1        |                |                   |                  |              |                  |               |                 | 0XE0    |
| 0xB5    | PR_VALUE2      | PR_VALUE2        |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xB6    | Reserved       | Reserved         |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xB7    | Reserved       | Reserved         |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xB8    | SPK_NG_CTRL1   | Reserved         | NG_EN          | NG_VTH            |                  |              | NG_ATK           |               |                 | 0X22    |
| 0xB9    | SPK_NG_CTRL2   | ANA_SETUP_DLY_EN | CLK_FAULT_MODE | NG_ON_FALLING_INT | NG_ON_RISING_INT | ENV_RST_TRIM | INT_I2C_LATCH_EN | NG_SOURCE_SEL |                 | 0X87    |
| 0xBA    | DGC_1          | ATTACK_DGC       |                |                   | TIMEOUT_DGC      |              | DGC_REF_TEST_EN  | ZCR_EN        | DGC_EN          | 0X82    |
| 0xBB    | DGC_2          | DGC_THR          |                |                   |                  |              |                  |               | DGC_THR_TEST_EN | 0X41    |
| 0xBC    | DGC_3          | DGC_DLY          |                |                   |                  |              |                  |               |                 | 0X94    |
| 0xBD    | MCBS_CTRL1     | Reserved         |                | MCBS_MODE         | MCBS_EN          | MCBS_DEV1    |                  |               | 0X00            |         |
| 0xBE    | MCBS_CTRL2     | MCBS_DEV2        |                |                   |                  | MCBS_DEV3    |                  |               |                 | 0X00    |
| 0xF5    | Ready_for_VBAT | READY_FOR_VBAT   |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xF7    | Ready_for_TEMP | READY_FOR_TEMP   |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xF8    | Status_T1      | Reserved         |                |                   |                  | TEMP_MON_MSB |                  |               |                 | 0X00    |
| 0xF9    | Status_T2      | TEMP_MON_LSB     |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xFA    | Status1        | OT1_OK           | OT2_OK         | UVLO              | BST_OS           | POWER_F      | Reserved         |               | NG_ON           | 0XC0    |
| 0xFB    | Status2        | SCAN_CHK         | Reserved       | OCP_SPK           | OCP_BST          | BOP_STATE    |                  |               | CLOCK_MON       | 0X00    |
| 0xFC    | Status3        | Reserved         |                |                   |                  | VBAT_MON_MSB |                  |               |                 | 0X00    |
| 0xFD    | Status4        | VBAT_MON_LSB     |                |                   |                  |              |                  |               |                 | 0X00    |
| 0xFE    | Status5        | Reserved         |                |                   |                  |              |                  | INTN          | INT             | 0X02    |
| 0xFF    | Device_Index   | DEVICE_ID        |                |                   |                  |              | REV_NUM          |               |                 | 0X1A    |

### Clock Modes and Power-Up

| Register | Function   | Name                    | Bit |   |   |   |   |   |   |   | Description                                                                                                          |
|----------|------------|-------------------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------|
|          |            |                         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                      |
| 0x00     | SystemCTRL | -                       |     |   |   |   |   |   |   |   | Reserved                                                                                                             |
|          |            | RESETBYI <sup>2</sup> C |     |   |   |   |   |   |   |   | I <sup>2</sup> C Register Reset<br>0: Normal operation (keep I <sup>2</sup> C)<br>1: I <sup>2</sup> C register reset |
|          |            | POWERUP                 |     |   |   |   |   |   |   |   | Power-up<br>0: Power-down (I <sup>2</sup> C registers are alive)<br>1: Normal operation                              |
|          |            | Default                 | 1   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x80                                                                                                                 |

### Input Control

| Register | Function   | Name                  | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                  |
|----------|------------|-----------------------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |            |                       | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                              |
| 0x01     | InputCTRL1 | -                     |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                                                     |
|          |            | I <sup>2</sup> S MODE |     |   |   |   |   |   |   |   | I <sup>2</sup> S Input Format<br>000: Philips standard I <sup>2</sup> S<br>001: Left justified<br>010: Not used<br>011: Not used<br>100: Right justified 16-bit<br>101: Right justified 18-bit<br>110: Right justified 20-bit<br>111: Right justified 24-bit |
|          |            | LEFTPOL               |     |   |   |   |   |   |   |   | First-Channel Polarity for I <sup>2</sup> S<br>0: Low for first-channel data (I <sup>2</sup> S standard)<br>1: High for first-channel data                                                                                                                   |
|          |            | SCK_RISING            |     |   |   |   |   |   |   |   | Data Written on SCK Falling / Rising Edge for I <sup>2</sup> S and TDM<br>0: Data written on SCK falling edge (I <sup>2</sup> S standard)<br>1: Data written on SCK rising edge                                                                              |
|          |            | -                     |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                                                     |
|          |            | Default               | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                                                                                                                                                         |

**BOP\_1**

| Register | Function             | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                      |
|----------|----------------------|---------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------------------------------|
|          |                      |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                  |
| 0x02     | BrownOut Protection1 | BO_LVL1 |     |   |   |   |   |   |   |   | Brown Out LV1 Setting<br>Default 4.02 V<br>Level [V] = (BO_LVL1 / 256) * 6<br>(when VREF = 1.2V) |
|          |                      | Default | 0   | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0x6D                                                                                             |

| Register | Function             | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|----------------------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |                      |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0x03     | BrownOut Protection2 | BO_LVL2 |     |   |   |   |   |   |   |   | Brown Out LV2 Setting<br>Default 3.80 V<br>Level [V] = (BO_LVL2 / 256) * 6<br>(when VREF = 1.2 V) |
|          |                      | Default | 0   | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0x67                                                                                              |

| Register | Function             | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|----------------------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |                      |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0x04     | BrownOut Protection3 | BO_LVL3 |     |   |   |   |   |   |   |   | Brown Out LV3 Setting<br>Default 3.65 V<br>Level [V] = (BO_LVL3 / 256) * 6<br>(when VREF = 1.2 V) |
|          |                      | Default | 0   | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0x63                                                                                              |

| Register | Function             | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|----------------------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |                      |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0x05     | BrownOut Protection8 | BO_LVL4 |     |   |   |   |   |   |   |   | Brown Out LV4 Setting<br>Default 3.32 V<br>Level [V] = (BO_LVL4 / 256) * 6<br>(when VREF = 1.2 V) |
|          |                      | Default | 0   | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0x5A                                                                                              |

| Register | Function             | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|----------------------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |                      |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0x06     | BrownOut Protection9 | BO_LVL5 |     |   |   |   |   |   |   |   | Brown Out LV5 Setting<br>Default 3.10 V<br>Level [V] = (BO_LVL5 / 256) * 6<br>(when VREF = 1.2 V) |
|          |                      | Default | 0   | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0x54                                                                                              |

| Register | Function              | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|-----------------------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |                       |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0x07     | BrownOut Protection10 | BO_LVL6 |     |   |   |   |   |   |   |   | Brown Out LV6 Setting<br>Default 2.84 V<br>Level [V] = (BO_LVL6 / 256) * 6<br>(when VREF = 1.2 V) |
|          |                       | Default | 0   | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0x4D                                                                                              |

# SMA1857

| Register | Function              | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|-----------------------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |                       |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0x08     | BrownOut Protection11 | BO_LVL7 |     |   |   |   |   |   |   |   | Brown Out LV7 Setting<br>Default 2.76 V<br>Level [V] = (BO_LVL7 / 256) * 6<br>(when VREF = 1.2 V) |
|          |                       | Default | 0   | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0x4B                                                                                              |

## Output Control

| Register | Function   | Name         | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                                                                                       |
|----------|------------|--------------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |            |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                                                                                   |
| 0x09     | OutputCTRL | PORT_CONFIG  |     |   |   |   |   |   |   |   | Input / Output Port Configuration<br>00: Input port only<br>01: Reserved<br>10: Output port enable<br>11: Reserved                                                                                                                                                                                                                |
|          |            | SDO_OUT1_SEL |     |   |   |   |   |   |   |   | 000: Disable<br>001: Format converter<br>010: Mono mixer output<br>(0x11[4], 0x11[0] bits are related)<br>011: Speaker path after DSP<br>100: Vrms^2_average<br>/ MCBS_IN(If REGBD[4] is high, MCBS_IN is selected)<br>101: Battery monitoring<br>110: Temperature monitoring<br>111: Speaker path<br>(after DSP, POSTVOL, DELAY) |
|          |            | SDO_OUT0_SEL |     |   |   |   |   |   |   |   | 000: Disable<br>001: Format converter<br>010: Mono mixer output<br>(0x11[4], 0x11[0] bits are related)<br>011: Speaker path after DSP<br>100: Vrms^2_average<br>/ MCBS_IN(If REGBD[4] is high, MCBS_IN is selected)<br>101: Battery monitoring<br>110: Temperature monitoring<br>111: Speaker path<br>(after DSP, POSTVOL, DELAY) |
|          |            | Default      | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                                                                                                                                                                                                                              |

## Volume Control

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description                                                                    |
|----------|----------|---------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                |
| 0x0A     | SPK_VOL  | SPKVOL  |     |   |   |   |   |   |   |   | Speaker Channel Volume (default -20 dB)<br>-0.5 dB steps. See the volume table |
|          |          | Default | 0   | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0x58                                                                           |

**Amplifier Channel Volume Table**

| Register Value | Gain (dB) | Register Value | Gain (dB) | Register Value | Gain (dB) | Register Value | Gain (dB) |
|----------------|-----------|----------------|-----------|----------------|-----------|----------------|-----------|
| 0x00           | 24.0      | 0x2B           | 2.5       | 0x56           | -19.0     | 0x81           | -40.5     |
| 0x01           | 23.5      | 0x2C           | 2.0       | 0x57           | -19.5     | 0x82           | -41.0     |
| 0x02           | 23.0      | 0x2D           | 1.5       | 0x58           | -20.0     | 0x83           | -41.5     |
| 0x03           | 22.5      | 0x2E           | 1.0       | 0x59           | -20.5     | 0x84           | -42.0     |
| 0x04           | 22.0      | 0x2F           | 0.5       | 0x5A           | -21.0     | 0x85           | -42.5     |
| 0x05           | 21.5      | 0x30           | 0.0       | 0x5B           | -21.5     | 0x86           | -43.0     |
| 0x06           | 21.0      | 0x31           | -0.5      | 0x5C           | -22.0     | 0x87           | -43.5     |
| 0x07           | 20.5      | 0x32           | -1.0      | 0x5D           | -22.5     | 0x88           | -44.0     |
| 0x08           | 20.0      | 0x33           | -1.5      | 0x5E           | -23.0     | 0x89           | -44.5     |
| 0x09           | 19.5      | 0x34           | -2.0      | 0x5F           | -23.5     | 0x8A           | -45.0     |
| 0x0A           | 19.0      | 0x35           | -2.5      | 0x60           | -24.0     | 0x8B           | -45.5     |
| 0x0B           | 18.5      | 0x36           | -3.0      | 0x61           | -24.5     | 0x8C           | -46.0     |
| 0x0C           | 18.0      | 0x37           | -3.5      | 0x62           | -25.0     | 0x8D           | -46.5     |
| 0x0D           | 17.5      | 0x38           | -4.0      | 0x63           | -25.5     | 0x8E           | -47.0     |
| 0x0E           | 17.0      | 0x39           | -4.5      | 0x64           | -26.0     | 0x8F           | -47.5     |
| 0x0F           | 16.5      | 0x3A           | -5.0      | 0x65           | -26.5     | 0x90           | -48.0     |
| 0x10           | 16.0      | 0x3B           | -5.5      | 0x66           | -27.0     | 0x91           | -48.5     |
| 0x11           | 15.5      | 0x3C           | -6.0      | 0x67           | -27.5     | 0x92           | -49.0     |
| 0x12           | 15.0      | 0x3D           | -6.5      | 0x68           | -28.0     | 0x93           | -49.5     |
| 0x13           | 14.5      | 0x3E           | -7.0      | 0x69           | -28.5     | 0x94           | -50.0     |
| 0x14           | 14.0      | 0x3F           | -7.5      | 0x6A           | -29.0     | 0x95           | -50.5     |
| 0x15           | 13.5      | 0x40           | -8.0      | 0x6B           | -29.5     | 0x96           | -51.0     |
| 0x16           | 13.0      | 0x41           | -8.5      | 0x6C           | -30.0     | 0x97           | -51.5     |
| 0x17           | 12.5      | 0x42           | -9.0      | 0x6D           | -30.5     | 0x98           | -52.0     |
| 0x18           | 12.0      | 0x43           | -9.5      | 0x6E           | -31.0     | 0x99           | -52.5     |
| 0x19           | 11.5      | 0x44           | -10.0     | 0x6F           | -31.5     | 0x9A           | -53.0     |
| 0x1A           | 11.0      | 0x45           | -10.5     | 0x70           | -32.0     | 0x9B           | -53.5     |
| 0x1B           | 10.5      | 0x46           | -11.0     | 0x71           | -32.5     | 0x9C           | -54.0     |
| 0x1C           | 10.0      | 0x47           | -11.5     | 0x72           | -33.0     | 0x9D           | -54.5     |
| 0x1D           | 9.5       | 0x48           | -12.0     | 0x73           | -33.5     | 0x9E           | -55.0     |
| 0x1E           | 9.0       | 0x49           | -12.5     | 0x74           | -34.0     | 0x9F           | -55.5     |
| 0x1F           | 8.5       | 0x4A           | -13.0     | 0x75           | -34.5     | 0xA0           | -56.0     |
| 0x20           | 8.0       | 0x4B           | -13.5     | 0x76           | -35.0     | 0xA1           | -56.5     |
| 0x21           | 7.5       | 0x4C           | -14.0     | 0x77           | -35.5     | 0xA2           | -57.0     |
| 0x22           | 7.0       | 0x4D           | -14.5     | 0x78           | -36.0     | 0xA3           | -57.5     |
| 0x23           | 6.5       | 0x4E           | -15.0     | 0x79           | -36.5     | 0xA4           | -58.0     |
| 0x24           | 6.0       | 0x4F           | -15.5     | 0x7A           | -37.0     | 0xA5           | -58.5     |
| 0x25           | 5.5       | 0x50           | -16.0     | 0x7B           | -37.5     | 0xA6           | -59.0     |
| 0x26           | 5.0       | 0x51           | -16.5     | 0x7C           | -38.0     | 0xA7           | -59.5     |
| 0x27           | 4.5       | 0x52           | -17.0     | 0x7D           | -38.5     | 0xA8           | -∞        |
| 0x28           | 4.0       | 0x53           | -17.5     | 0x7E           | -39.0     | ...            | ...       |
| 0x29           | 3.5       | 0x54           | -18.0     | 0x7F           | -39.5     | ...            | ...       |
| 0x2A           | 3.0       | 0x55           | -18.5     | 0x80           | -40.0     | 0xFF           | -∞        |

### Mute Control

| Register | Function      | Name       | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                           |
|----------|---------------|------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |               |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                       |
| 0x0E     | MUTE_VOL_CTRL | VOL_SLOPE  |     |   |   |   |   |   |   |   | Fs = 48 kHz, volume > -60 dB<br>00: Off<br>01: Slow(approximately)<br>1.3 ms / 0.5 dB<br>10: Medium(approximately)<br>0.82 ms / 0.5 dB<br>11: Fast(approximately)<br>0.41 ms / 0.5 dB |
|          |               | MUTE_SLOPE |     |   |   |   |   |   |   |   | Fs = 48 kHz, volume > -60 dB<br>00: Off<br>01: (approximately) 200 ms / -20 dB<br>10: (approximately) 50 ms / -20 dB<br>11: (approximately) 10 ms / -20 dB                            |
|          |               | -          |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                              |
|          |               | SPK_MUTE   |     |   |   |   |   |   |   |   | 0: Signal path un-muted<br>1: Signal path muted                                                                                                                                       |
|          |               | Default    | 1   | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0xAF                                                                                                                                                                                  |

### VBAT AND TEMPERATURE SENSING CONTROL

| Register | Function          | Name          | Bit |   |   |   |   |   |   |   | Description                                                                                 |
|----------|-------------------|---------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------|
|          |                   |               | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                             |
| 0x0F     | VBAT_TEMP_SENSING | SENSING_PD    |     |   |   |   |   |   |   |   | VBAT & Temperature Sensing Operation<br>0: On<br>1: Off                                     |
|          |                   | VBAT_LPF_BYP  |     |   |   |   |   |   |   |   | VBAT LPF Bypass<br>00: Activate LPF<br>11: Bypass LPF (LPF power down)<br>01,10: Do not use |
|          |                   | -             |     |   |   |   |   |   |   |   | Reserved                                                                                    |
|          |                   | CLK_FREQUENCY |     |   |   |   |   |   |   |   | Sampling Frequency Control<br>00: 3 kHz (default)<br>01: 6 kHz<br>10: 12 kHz<br>11: 24 kHz  |
|          |                   | Default       | 1   | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0xE0                                                                                        |

**System Control**

| Register | Function    | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                |
|----------|-------------|---------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |             |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                            |
| 0x10     | SystemCTRL1 | -       |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                   |
|          |             | SPKMODE |     |   |   |   |   |   |   |   | Speaker Mode<br>000: Off (default)<br>001: Mono for one chip solution<br>010 to 011: Reserved<br>100: Stereo for two chip solution<br>101 to 111: Reserved |
|          |             | -       |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                   |
|          |             | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                                                       |

| Register | Function    | Name       | Bit |   |   |   |   |   |   |   | Description                                                                |
|----------|-------------|------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------|
|          |             |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                            |
| 0x11     | SystemCTRL2 | -          |     |   |   |   |   |   |   |   | Reserved                                                                   |
|          |             | SPKSET     |     |   |   |   |   |   |   |   | Bass<br>0: Bypass<br>1: Enable                                             |
|          |             |            |     |   |   |   |   |   |   |   | Comp / Limiter<br>0: Bypass<br>1: Enable                                   |
|          |             | LR_DATA_SW |     |   |   |   |   |   |   |   | LR_DATA_SW<br>0: Normal<br>1: Left / right data swap for two chip solution |
|          |             | -          |     |   |   |   |   |   |   |   | Reserved                                                                   |
|          |             | MONO_MIX   |     |   |   |   |   |   |   |   | Mono Mix<br>0: Disable<br>1: Enable                                        |
|          |             | Default    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                       |

| Register | Function    | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                                                          |
|----------|-------------|---------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------------------------------------------------------------------|
|          |             |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                      |
| 0x12     | SystemCTRL3 | INPUT   |     |   |   |   |   |   |   |   | Input Gain<br>00: 0 dB<br>01: -6 dB<br>10: -12 dB<br>11: -∞ dB                                                                       |
|          |             | INPUT_R |     |   |   |   |   |   |   |   | Input Gain for Right Channel<br>(this setting is valid in I <sup>2</sup> S mode)<br>00: 0 dB<br>01: -6 dB<br>10: -12 dB<br>11: -∞ dB |
|          |             | -       |     |   |   |   |   |   |   |   | Reserved                                                                                                                             |
|          |             | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                                 |

## Delay

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------|----------|---------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 0x13     | DELAY    | -       |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|          |          | BYP_DLY |     |   |   |   |   |   |   |   | Bypass Delay<br>0: Delay On<br>(delay time is set by SET_DLY, 0x13[3:0])<br>1: Bypass                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|          |          | SET_DLY |     |   |   |   |   |   |   |   | Delay Setting<br>0000: 2 x Ts, 41.67 $\mu$ sec<br>0001: 3 x Ts, 62.50 $\mu$ sec<br>0010: 4 x Ts, 83.33 $\mu$ sec<br>0011: 5 x Ts, 104.17 $\mu$ sec<br>0100: 6 x Ts, 125.00 $\mu$ sec<br>0101: 7 x Ts, 145.83 $\mu$ sec<br>0110: 8 x Ts, 166.67 $\mu$ sec<br>0111: 9 x Ts, 187.50 $\mu$ sec<br>1000: 10 x Ts, 208.33 $\mu$ sec<br>1001: 11 x Ts, 229.17 $\mu$ sec<br>1010: 12 x Ts, 250.00 $\mu$ sec<br>1011: 13 x Ts, 270.83 $\mu$ sec<br>1100: 14 x Ts, 291.67 $\mu$ sec<br>1101: 15 x Ts, 312.50 $\mu$ sec<br>1110: 16 x Ts, 333.33 $\mu$ sec<br>1111: 17 x Ts, 354.17 $\mu$ sec |
|          |          | Default | 0   | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0x09                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

## Modulator

| Register | Function  | Name       | Bit |   |   |   |   |   |   |   | Description                                                                                           |
|----------|-----------|------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------|
|          |           |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                       |
| 0x14     | Modulator | SPK_HYSFB  |     |   |   |   |   |   |   |   | 00: 625 kHz<br>01: 414 kHz<br>10: 297 kHz<br>11: 226 kHz                                              |
|          |           | SPK_BDELAY |     |   |   |   |   |   |   |   | 00_0000 to 11_1111: Delay control<br>between OUTA and OUTB with main clock<br>duty cycle (24.576 MHz) |
|          |           | Default    | 0   | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0x60                                                                                                  |

**BassBoost**

| Register | Function | Name         | Bit |   |   |   |   |   |   |   | Description                   |
|----------|----------|--------------|-----|---|---|---|---|---|---|---|-------------------------------|
|          |          |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                               |
| 0x15     | BassSpk1 | S BSPK_F0A_M |     |   |   |   |   |   |   |   | SBSpk_F0A[9:2] Q0.10 unsigned |
|          |          | Default      | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x01                          |

| Register | Function | Name          | Bit |   |   |   |   |   |   |   | Description                     |
|----------|----------|---------------|-----|---|---|---|---|---|---|---|---------------------------------|
|          |          |               | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                 |
| 0x16     | BassSpk2 | S BSPK_F0B1_M |     |   |   |   |   |   |   |   | SBSpk_F0B1[10:3] Q1.10 unsigned |
|          |          | Default       | 0   | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0x0F                            |

| Register | Function | Name          | Bit |   |   |   |   |   |   |   | Description                     |
|----------|----------|---------------|-----|---|---|---|---|---|---|---|---------------------------------|
|          |          |               | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                 |
| 0x17     | BassSpk3 | S BSPK_F0B2_M |     |   |   |   |   |   |   |   | SBSpk_F0B1[10:3] Q1.10 unsigned |
|          |          | Default       | 0   | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0x0F                            |

| Register | Function | Name         | Bit |   |   |   |   |   |   |   | Description                     |
|----------|----------|--------------|-----|---|---|---|---|---|---|---|---------------------------------|
|          |          |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                 |
| 0x18     | BassSpk4 | S BSPK_F0C_M |     |   |   |   |   |   |   |   | SBSpk_F0B1[10:3] Q0.10 unsigned |
|          |          | Default      | 0   | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0x0F                            |

| Register | Function | Name        | Bit |   |   |   |   |   |   |   | Description                                                                                                   |
|----------|----------|-------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------|
|          |          |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                               |
| 0x19     | BassSpk5 | -           |     |   |   |   |   |   |   |   | Reserved                                                                                                      |
|          |          | S BSPK_LSB1 |     |   |   |   |   |   |   |   | SBSpk_F0A[1:0] Q0.10 unsigned                                                                                 |
|          |          |             |     |   |   |   |   |   |   |   | SBSpk_F0B1[2:0] Q1.10 unsigned                                                                                |
|          |          | S BSPKGAIN  |     |   |   |   |   |   |   |   | 00: Lowest +3.5 dB (1 + 0.5)<br>01: Low +6 dB (1 + 1)<br>10: High +9 dB (1 + 2)<br>11: Highest +14 dB (1 + 4) |
|          |          |             |     |   |   |   |   |   |   |   |                                                                                                               |
|          |          | Default     | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                          |

| Register | Function | Name        | Bit |   |   |   |   |   |   |   | Description                                          |
|----------|----------|-------------|-----|---|---|---|---|---|---|---|------------------------------------------------------|
|          |          |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                      |
| 0x1A     | BassSpk6 | -           |     |   |   |   |   |   |   |   | Reserved                                             |
|          |          | S BSPK_LSB2 |     |   |   |   |   |   |   |   | SB_F0B2[2:0] Q1.10 unsigned                          |
|          |          |             |     |   |   |   |   |   |   |   | SB_F0C[1:0] Q0.10 unsigned                           |
|          |          | S BSPKTHRES |     |   |   |   |   |   |   |   | 00: -40 dB<br>01: -26 dB<br>10: -20 dB<br>11: -14 dB |
|          |          |             |     |   |   |   |   |   |   |   |                                                      |
|          |          | Default     | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                 |

## SMA1857

| Register | Function | Name         | Bit |   |   |   |   |   |   |   | Description                                                                               |
|----------|----------|--------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------|
|          |          |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                           |
| 0x1B     | BassSpk7 | -            |     |   |   |   |   |   |   |   | Reserved                                                                                  |
|          |          | SBSPKTIME    |     |   |   |   |   |   |   |   | Attack Release Time of Bass<br>00: Long<br>01: Medium<br>10: Short<br>11: Reserved        |
|          |          | SBSPKFB_TYPE |     |   |   |   |   |   |   |   | Filter B Configuration<br>0: Low pass<br>1: Band pass                                     |
|          |          | SBSPKSEL     |     |   |   |   |   |   |   |   | Filter B Input Selection<br>0: Filter B through filter A<br>1: Filter B direct from input |
|          |          | Default      | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                      |

### BOP\_2

| Register | Function              | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|-----------------------|-----------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |                       |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0x1C     | BrownOut Protection20 | -         |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                                                                                                                                                                                             |
|          |                       | HOLD_TIME |     |   |   |   |   |   |   |   | Transition Time from State to State<br>0000: 0 $\mu$ sec (hold time skip)<br>0001: 10 $\mu$ sec<br>0010: 20 $\mu$ sec<br>0011: 40 $\mu$ sec<br>0100: 80 $\mu$ sec<br>0101: 160 $\mu$ sec<br>0110: 320 $\mu$ sec<br>0111: 640 $\mu$ sec<br>1000: 1.28 msec<br>1001: 2.56 msec<br>1010: 5.12 msec<br>1011: 10.24 msec<br>1100: 20.48 msec<br>1101: 40.96 msec<br>1110: 81.92 msec<br>1111: 163.84 msec |
|          |                       | Default   | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                                                                                                                                                                                                                                                                                                 |

| Register | Function             | Name    | Bit |   |   |   |   |   |   |   | Description                                                         |
|----------|----------------------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------|
|          |                      |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                     |
| 0x1D     | BrownOut Protection0 | BOP_PDN |     |   |   |   |   |   |   |   | Operation of Brown Out Protection<br>0: Power down<br>1: Enable BOP |
|          |                      | -       |     |   |   |   |   |   |   |   | Reserved                                                            |
|          |                      | BO_HYS  |     |   |   |   |   |   |   |   | Brown out hysteresis                                                |
|          |                      | Default | 0   | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0x08                                                                |

**Tone Generator**

| Register | Function       | Name              | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                                  |
|----------|----------------|-------------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |                |                   | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                              |
| 0x1E     | TONE_GENERATOR | -                 |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                                                                     |
|          |                | BYP_TONE_FINE     |     |   |   |   |   |   |   |   | Bypass Tone Generator and Fine Volume<br>0: Activate<br>1: Bypass                                                                                                                                                                                                            |
|          |                | TONE_AUDIO_MIX_ON |     |   |   |   |   |   |   |   | Tone Audio Mixing<br>0: MIX disable (tone only)<br>FINE_VOL*(TONE)<br>1: MIX enable<br>FINE_VOL*(TONE + AUDIO)                                                                                                                                                               |
|          |                | TONE_FREQ         |     |   |   |   |   |   |   |   | Tone Frequency<br>0000: 50 Hz<br>0001: 60 Hz<br>0010: 140 Hz<br>0011: 150 Hz<br>0100: 175 Hz<br>0101: 180 Hz<br>0110: 200 Hz<br>0111: 375 Hz<br>1000: 750 Hz<br>1001: 1 kHz<br>1010: 3 kHz<br>1011: 6 kHz<br>1100: 11.75 kHz<br>1101: 15 kHz<br>1110: 17 kHz<br>1111: 19 kHz |
|          |                | TONE_ON           |     |   |   |   |   |   |   |   | Tone Generator Enable<br>0: Tone generator off<br>1: Tone generator on                                                                                                                                                                                                       |
|          |                | Default           | 1   | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0xA1                                                                                                                                                                                                                                                                         |

| Register | Function          | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-------------------|----------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |                   |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 0x1F     | TONE/ FINE VOLUME | FINE_VOL |     |   |   |   |   |   |   |   | Fine Volume<br>0_0000: 3 dB<br>0_0001: 2.875 dB<br>0_0010: 2.75 dB<br>0_0011: 2.625 dB<br>0_0100: 2 dB<br>0_0101: 1.875 dB<br>0_0110: 1.75 dB<br>0_0111: 1.625 dB<br>0_1000: 1 dB<br>0_1001: 0.875 dB<br>0_1010: 0.75 dB<br>0_1011: 0.625 dB<br>0_1100: 0 dB<br>0_1101: -0.125 dB<br>0_1110: -0.250 dB<br>0_1111: -0.375 dB<br>1_0000: -1 dB<br>1_0001: -1.125 dB<br>1_0010: -1.25 dB<br>1_0011: -1.375 dB<br>1_0100: -2 dB |

|  |  |          |   |   |   |   |   |   |   |   |                                                                                                                                                                     |
|--|--|----------|---|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  |          |   |   |   |   |   |   |   |   | 1_0101: -2.125 dB<br>1_0110: -2.25 dB<br>1_0111: -2.375 dB<br>1_1000: -3 dB<br>1_1001: -3.125 dB<br>1_1010: -3.25 dB<br>1_1011: -3.375 dB<br>1_1100 to 1_1111: 0 dB |
|  |  | TONE_VOL |   |   |   |   |   |   |   |   | Tone Volume<br>000: 0 dB<br>001: -6 dB<br>010: -12 dB<br>011: -18 dB<br>100: -24 dB<br>101: -30 dB<br>110: -36 dB<br>111: Tone off<br>TONE_VOL*(TONE)               |
|  |  | Default  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0x67                                                                                                                                                                |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x20     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x21     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 1   | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0xAA        |

## COMLIM

| Register | Function          | Name         | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                      |
|----------|-------------------|--------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |                   |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                  |
| 0x22     | COMP_HYS Selector | -            |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                         |
|          |                   | COMP_HYS_SEL |     |   |   |   |   |   |   |   | DRC Hysteresis Selector<br>000: No hysteresis<br>001: 0.0625dB<br>010: 0.125dB<br>011: 0.1875dB<br>100: 0.25dB<br>101: 0.3125dB<br>110: 0.375dB<br>111: 0.4375dB |
|          |                   | Default      | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                                                             |

| Register | Function | Name          | Bit |   |   |   |   |   |   |   | Description                                                            |
|----------|----------|---------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------|
|          |          |               | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                        |
| 0x23     | CompLim1 | SPK_RATIO     |     |   |   |   |   |   |   |   | 0: 2:1<br>1: 4:1                                                       |
|          |          | SPK_HRD LIMIT |     |   |   |   |   |   |   |   | 00: 0.984375 FS (default)<br>01: 0.875 FS<br>10: 0.75 FS<br>11: 0.5 FS |

## SMA1857

|  |  |            |   |   |   |   |   |   |   |   |                                                                                                                                                                                   |
|--|--|------------|---|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  | SPK_LIMTHR |   |   |   |   |   |   |   |   | 00000: $-\infty$<br>00001: 1/32 = -30.1 dB<br>00010: 2/32 = -24.8 dB<br>.....<br>11001: 25/32 = -2.14 dB (default)<br>.....<br>11110: 30/32 = -0.56 dB<br>11111: 31/32 = -0.28 dB |
|  |  | Default    | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0x1F                                                                                                                                                                              |

| Register | Function | Name       | Bit |   |   |   |   |   |   |   | Description                                                          |
|----------|----------|------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------|
|          |          |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                      |
| 0x24     | CompLim2 | SPK_LIMATT |     |   |   |   |   |   |   |   | 0000: Shortest (default)<br>0001:<br>.....<br>1110:<br>1111: Longest |
|          |          | SPK_LIMREL |     |   |   |   |   |   |   |   | 0000: Shortest (default)<br>0001:<br>.....<br>1110:<br>1111: Longest |
|          |          | Default    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                 |

| Register | Function | Name       | Bit |   |   |   |   |   |   |   | Description                                                          |
|----------|----------|------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------|
|          |          |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                      |
| 0x25     | CompLim3 | SPK_COMATT |     |   |   |   |   |   |   |   | 0000: Shortest (default)<br>0001:<br>.....<br>1110:<br>1111: Longest |
|          |          | SPK_COMREL |     |   |   |   |   |   |   |   | 0000: Shortest (default)<br>0001:<br>.....<br>1110:<br>1111: Longest |
|          |          | Default    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                 |

| Register | Function | Name          | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                 |
|----------|----------|---------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |               | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                             |
| 0x26     | CompLim4 | SPK_COM THRES |     |   |   |   |   |   |   |   | 00000000: $-\infty$<br>00000001: 1/256 = -48 dB<br>00000010: 2/256 = -42 dB<br>.....<br>00000100: 4/256 = -30 dB (default)<br>.....<br>11111110: 254/256 = -0.07 dB<br>11111111: 255/256 = (compressor off) |
|          |          | Default       | 0   | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0x04                                                                                                                                                                                                        |

**BOP\_3**

| Register | Function             | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                                                         |
|----------|----------------------|----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------|
|          |                      |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                     |
| 0x27     | BrownOut Protection4 | BOP_LVL1 |     |   |   |   |   |   |   |   | Boost Current Limit = SET_OCL*BOP_LVL<br>BOP_LVL :<br>000: 1.0x            001: 0.9x<br>010: 0.8x            100: 0.6x<br>100: 0.3x |
|          |                      | LIM_THR1 |     |   |   |   |   |   |   |   | Limiter threshold 1<br>(see 0x23 CompLim1[4:0] SPK_LIMTHR*<br>register formula)<br>-1.16 dB                                         |
|          |                      | Default  | 0   | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0x1C                                                                                                                                |

| Register | Function             | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                                                         |
|----------|----------------------|----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------|
|          |                      |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                     |
| 0x28     | BrownOut Protection5 | BOP_LVL2 |     |   |   |   |   |   |   |   | Boost Current Limit = SET_OCL*BOP_LVL<br>BOP_LVL :<br>000: 1.0x            001: 0.9x<br>010: 0.8x            100: 0.6x<br>100: 0.3x |
|          |                      | LIM_THR2 |     |   |   |   |   |   |   |   | Limiter Threshold 2<br>(see 0x23 CompLim1[4:0] SPK_LIMTHR<br>register formula)<br>-1.47 dB                                          |
|          |                      | Default  | 0   | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0x1B                                                                                                                                |

| Register | Function              | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                                                         |
|----------|-----------------------|----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------|
|          |                       |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                     |
| 0x29     | BrownOut Protection12 | BOP_LVL3 |     |   |   |   |   |   |   |   | Boost Current Limit = SET_OCL*BOP_LVL<br>BOP_LVL :<br>000: 1.0x            001: 0.9x<br>010: 0.8x            100: 0.6x<br>100: 0.3x |
|          |                       | LIM_THR3 |     |   |   |   |   |   |   |   | Limiter Threshold 3<br>(see 0x23 CompLim1 [4:0] SPK_LIMTHR<br>register formula)<br>-2.49 dB                                         |
|          |                       | Default  | 0   | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0x18                                                                                                                                |

| Register | Function              | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                                                         |
|----------|-----------------------|----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------|
|          |                       |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                     |
| 0x2A     | BrownOut Protection13 | BOP_LVL4 |     |   |   |   |   |   |   |   | Boost Current Limit = SET_OCL*BOP_LVL<br>BOP_LVL :<br>000: 1.0x            001: 0.9x<br>010: 0.8x            100: 0.6x<br>100: 0.3x |
|          |                       | LIM_THR4 |     |   |   |   |   |   |   |   | Limiter Threshold 4<br>(see 0x23 CompLim1[4:0] SPK_LIMTHR<br>register formula)<br>-3.25 dB                                          |
|          |                       | Default  | 0   | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0x76                                                                                                                                |

# SMA1857

| Register | Function              | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                                                         |
|----------|-----------------------|----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------|
|          |                       |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                     |
| 0x2B     | BrownOut Protection14 | BOP_LVL5 |     |   |   |   |   |   |   |   | Boost Current Limit = SET_OCL*BOP_LVL<br>BOP_LVL :<br>000: 1.0x            001: 0.9x<br>010: 0.8x            100: 0.6x<br>100: 0.3x |
|          |                       | LIM_THR5 |     |   |   |   |   |   |   |   | Limiter Threshold 5<br>(see 0x23 CompLim1[4:0] SPK_LIMTHR register formula)<br>-4.08 dB                                             |
|          |                       | Default  | 1   | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0x94                                                                                                                                |

| Register | Function              | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                                                         |
|----------|-----------------------|----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------|
|          |                       |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                     |
| 0x2C     | BrownOut Protection15 | BOP_LVL6 |     |   |   |   |   |   |   |   | Boost Current Limit = SET_OCL*BOP_LVL<br>BOP_LVL :<br>000: 1.0x            001: 0.9x<br>010: 0.8x            100: 0.6x<br>100: 0.3x |
|          |                       | LIM_THR6 |     |   |   |   |   |   |   |   | Limiter Threshold 6<br>(see 0x23 CompLim1[4:0] SPK_LIMTHR register formula)<br>-4.5 dB                                              |
|          |                       | Default  | 1   | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0xB3                                                                                                                                |

| Register | Function             | Name        | Bit |   |   |   |   |   |   |   | Description                                                              |
|----------|----------------------|-------------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------|
|          |                      |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                          |
| 0x2D     | BrownOut Protection6 | COMP_THRES1 |     |   |   |   |   |   |   |   | Compress Threshold 1<br>(see 0x26 CompLim4 register formula)<br>-0.93 dB |
|          |                      | Default     | 1   | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0xE6                                                                     |

| Register | Function             | Name        | Bit |   |   |   |   |   |   |   | Description                                                              |
|----------|----------------------|-------------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------|
|          |                      |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                          |
| 0x2E     | BrownOut Protection7 | COMP_THRES2 |     |   |   |   |   |   |   |   | Compress Threshold 2<br>(see 0x26 CompLim4 register formula)<br>-1.41 dB |
|          |                      | Default     | 1   | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0xD9                                                                     |

| Register | Function              | Name        | Bit |   |   |   |   |   |   |   | Description                                                             |
|----------|-----------------------|-------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------|
|          |                       |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                         |
| 0x2F     | BrownOut Protection16 | COMP_THRES3 |     |   |   |   |   |   |   |   | Compress Threshold 3<br>(see 0x26 CompLim4 register formula)<br>-2.5 dB |
|          |                       | Default     | 1   | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0xC0                                                                    |

## SMA1857

| Register | Function              | Name        | Bit |   |   |   |   |   |   |   | Description                                                             |
|----------|-----------------------|-------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------|
|          |                       |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                         |
| 0x30     | BrownOut Protection17 | COMP_THRES4 |     |   |   |   |   |   |   |   | Compress Threshold 4<br>(see 0x26 CompLim4 register formula)<br>-3.1 dB |
|          |                       | Default     | 1   | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0xB3                                                                    |

| Register | Function              | Name        | Bit |   |   |   |   |   |   |   | Description                                                             |
|----------|-----------------------|-------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------|
|          |                       |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                         |
| 0x31     | BrownOut Protection18 | COMP_THRES5 |     |   |   |   |   |   |   |   | Compress Threshold 5<br>(see 0x26 CompLim4 register formula)<br>-3.7 dB |
|          |                       | Default     | 1   | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0xA6                                                                    |

| Register | Function              | Name        | Bit |   |   |   |   |   |   |   | Description                                                             |
|----------|-----------------------|-------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------|
|          |                       |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                         |
| 0x32     | BrownOut Protection19 | COMP_THRES6 |     |   |   |   |   |   |   |   | Compress Threshold 6<br>(see 0x26 CompLim4 register formula)<br>-4.5 dB |
|          |                       | Default     | 1   | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0x99                                                                    |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x33     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

### Analog Settings\_1

| Register | Function | Name       | Bit |   |   |   |   |   |   |   | Description                                                               |
|----------|----------|------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------|
|          |          |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                           |
| 0x34     | OCP_SPK  | -          |     |   |   |   |   |   |   |   | Reserved                                                                  |
|          |          | OCP_FILTER |     |   |   |   |   |   |   |   | Filter Time<br>00: Slowest<br>.....<br>11: Fastest                        |
|          |          | OCP_LVL_N  |     |   |   |   |   |   |   |   | Speaker OCP Level<br>00: 1.7 A      01: 2.0 A<br>10: 2.4 A      11: 2.7 A |
|          |          | Default    | 0   | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0x09                                                                      |

| Register | Function       | Name  | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                    |
|----------|----------------|-------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |                |       | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                |
| 0x35     | FDPEC Control0 | I_OP1 |     |   |   |   |   |   |   |   | OP1 Current Control (normal mode / low power mode (0x3F[3] : LOW_PWR))<br>00: 40 $\mu$ A / 20 $\mu$ A<br>01: 80 $\mu$ A / 40 $\mu$ A (default)<br>10: 120 $\mu$ A / 60 $\mu$ A<br>11: 160 $\mu$ A / 80 $\mu$ A |
|          |                | I_OP2 |     |   |   |   |   |   |   |   | OP2 Current Control<br>00: 30 $\mu$ A                                                                                                                                                                          |

# SMA1857

|  |  |            |   |   |   |   |   |   |   |                                                                                                                            |
|--|--|------------|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------|
|  |  |            |   |   |   |   |   |   |   | 01: 40 $\mu$ A (default)<br>10: 50 $\mu$ A<br>11: 60 $\mu$ A                                                               |
|  |  | AMP_RES    |   |   |   |   |   |   |   | SPK Amplifier Input Resistor, activated when 0x3F ATEST2[4] AMP_RES_MODE = 1<br>0: 16 k $\Omega$<br>1: 2 k $\Omega$        |
|  |  | SYNC_RESL  |   |   |   |   |   |   |   | Sync Resistor Selection<br>0: High R (64 k $\Omega$ )<br>1: Low R (10 k $\Omega$ )                                         |
|  |  | FDPEC_GAIN |   |   |   |   |   |   |   | SPK Amplifier Analog Loop Gain<br>00: RCV mode, x 0.5<br>01: RCV mode, x 1.1<br>10: SPK mode, x 3.0<br>11: SPK mode, x 3.6 |
|  |  | Default    | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0x56                                                                                                                       |

| Register | Function   | Name                 | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                    |
|----------|------------|----------------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |            |                      | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                |
| 0x36     | Protection | EGDE_DIS             |     |   |   |   |   |   |   |   | 0: Edge displacement enable<br>1: Edge displacement disable                                                                                                                                                    |
|          |            | LR_DELAY             |     |   |   |   |   |   |   |   |                                                                                                                                                                                                                |
|          |            | TEST_OCP_STEREO_MODE |     |   |   |   |   |   |   |   | Test mode set for stereo OCP MODE<br>0: OCP MODE is not valid at stereo<br>1: OCP_MODE is valid at stereo (default)                                                                                            |
|          |            | SPK_OCP_DIS          |     |   |   |   |   |   |   |   | 0: Overcurrent protection speaker output state enable<br>1: Overcurrent protection speaker output state disable                                                                                                |
|          |            | OCP_MODE             |     |   |   |   |   |   |   |   | 0: Auto recover (1 sec)<br>1: Permanent shutdown of output stage                                                                                                                                               |
|          |            | OTP_MODE             |     |   |   |   |   |   |   |   | Thermal Protection<br>00: Disable<br>01: Ignore threshod1, shutdown at threshold2<br>10: Reduced output power at threshold1, shutdown at threshold2<br>11: Shutdown chip at threshold1, shutdown at threshold2 |
|          |            | Default              | 1   | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0x92                                                                                                                                                                                                           |

| Register | Function  | Name          | Bit |   |   |   |   |   |   |   | Description                                          |
|----------|-----------|---------------|-----|---|---|---|---|---|---|---|------------------------------------------------------|
|          |           |               | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                      |
| 0x37     | SlopeCTRL | -             |     |   |   |   |   |   |   |   | Reserved                                             |
|          |           | SPK_SLOPE     |     |   |   |   |   |   |   |   | PWM Slope Control<br>00 (long) to 11 (short)         |
|          |           | SPK_DEAD TIME |     |   |   |   |   |   |   |   | PWM Dead Time Control<br>0000 (long) to 1111 (short) |
|          |           | Default       | 0   | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0x25                                                 |

**POWER METER**

| Register | Function   | Name     | Bit |   |   |   |   |   |   |   | Description                                                                                  |
|----------|------------|----------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------|
|          |            |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                              |
| 0x38     | PowerMeter | PMT_EN   |     |   |   |   |   |   |   |   | Power Meter Enable<br>0: Disable<br>1: Enable                                                |
|          |            | PMT_INI  |     |   |   |   |   |   |   |   | Operation Start Point<br>0: PR Value Input<br>1: Power Meter Enable                          |
|          |            | PMT_ATK  |     |   |   |   |   |   |   |   | Power Meter Level Attack Time<br>00: 10 msec<br>01: 20 msec<br>10: 40 msec<br>11: 80 msec    |
|          |            | PMT_REL  |     |   |   |   |   |   |   |   | Power Meter Level Release Time<br>00: 40 msec<br>01: 80 msec<br>10: 160 msec<br>11: 320 msec |
|          |            | NZ_VAL_1 |     |   |   |   |   |   |   |   | NZ_VAL [11:8] Neutral Zone Value MSB                                                         |
|          |            | Default  | 0   | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0x31                                                                                         |

| Register | Function   | Name     | Bit |   |   |   |   |   |   |   | Description                         |
|----------|------------|----------|-----|---|---|---|---|---|---|---|-------------------------------------|
|          |            |          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                     |
| 0x39     | PMT_NZ_VAL | NZ_VAL_2 |     |   |   |   |   |   |   |   | NZ_VAL [7:0] Neutral Zone Value LSB |
|          |            | Default  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x3A     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

**Analog Settings\_2**

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description                  |
|----------|----------|---------|-----|---|---|---|---|---|---|---|------------------------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                              |
| 0x3B     | Test1    | CODE    |     |   |   |   |   |   |   |   | 5 A : Enables test registers |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                         |

| Register | Function | Name         | Bit |   |   |   |   |   |   |   | Description                                                    |
|----------|----------|--------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------|
|          |          |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                |
| 0x3C     | Test2    | DIS_BSIDE    |     |   |   |   |   |   |   |   | 0: Bside enable<br>1: Bside disable                            |
|          |          | SDM_DC       |     |   |   |   |   |   |   |   | 0: Normal operation<br>1: DC test – DC value is set by volume. |
|          |          | SDM_SYNC_DIS |     |   |   |   |   |   |   |   | 0: Normal operation<br>1: LR sync disable                      |
|          |          | SPK_HSDM_BP  |     |   |   |   |   |   |   |   | 0: HSDM enable<br>1: HSDM bypass                               |
|          |          | SPK_OFF      |     |   |   |   |   |   |   |   | 0: Enable<br>1: Off                                            |
|          |          | -            |     |   |   |   |   |   |   |   | Reserved                                                       |
|          |          | Default      | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                           |

| Register | Function | Name           | Bit |   |   |   |   |   |   |   | Description                                                                              |
|----------|----------|----------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------|
|          |          |                | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                          |
| 0x3D     | Test3    | PWM_TIE_EN     |     |   |   |   |   |   |   |   | Digital Modulator Output Tie Enable<br>0: Tie Disable<br>1: Tie Enable                   |
|          |          | PWM_TIE_SEL    |     |   |   |   |   |   |   |   | Digital Modulator Output Tie Selection<br>0: A = 1'b1, B = 1'b0<br>1: A = 1'b0, B = 1'b1 |
|          |          | -              |     |   |   |   |   |   |   |   | Reserved                                                                                 |
|          |          | SPK_5050       |     |   |   |   |   |   |   |   | 0: Normal operation<br>1: Speaker 50% duty cycle enable, period set by volume.           |
|          |          | -              |     |   |   |   |   |   |   |   | Reserved                                                                                 |
|          |          | DC_CAL_DIS     |     |   |   |   |   |   |   |   | 0: DC calibration enable<br>1: DC calibration disable                                    |
|          |          | NG_DIR_CTRL_EN |     |   |   |   |   |   |   |   | Noise gate direct control<br>0: normal<br>1: noise gate direct enable                    |
|          |          | Default        | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                     |

| Register | Function                        | Name         | Bit |   |   |   |   |   |   |   | Description                                              |
|----------|---------------------------------|--------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------|
|          |                                 |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                          |
| 0x3E     | DIG_IDLE<br>CURRENT_<br>CONTROL | -            |     |   |   |   |   |   |   |   | Reserved                                                 |
|          |                                 | IDLE_TDM     |     |   |   |   |   |   |   |   | TDM_RX<br>1: Power down<br>0: Enable                     |
|          |                                 | IDLE_SYNC    |     |   |   |   |   |   |   |   | SYNC_DATA<br>1: Power down<br>0: Enable                  |
|          |                                 | IDLE_SOUT    |     |   |   |   |   |   |   |   | SOUT_TX<br>1: Power down<br>0: Enable                    |
|          |                                 | IDLE_RMS2    |     |   |   |   |   |   |   |   | RMS^2 Detector<br>1: Power down<br>0: Enable             |
|          |                                 | IDLE_ENV     |     |   |   |   |   |   |   |   | ENV_TRA<br>1: Power down<br>0: Enable                    |
|          |                                 | IDLE_BOP     |     |   |   |   |   |   |   |   | BOP_CTRL<br>1: Power down<br>0: Enable                   |
|          |                                 | IDLE_PLLTEST |     |   |   |   |   |   |   |   | PLL for Test<br>1: Power down<br>0: PLL Test Mode Enable |
|          |                                 | Default      | 0   | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0x09                                                     |

| Register | Function | Name         | Bit |   |   |   |   |   |   |   | Description                                                                                                                                 |
|----------|----------|--------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                             |
| 0x3F     | ATEST2   | VREF_TEST    |     |   |   |   |   |   |   |   | Analog VREF Mode<br>0: Off at Noise Gate Mode (PWM off)<br>1: On at Noise Gate Mode (PWM off)                                               |
|          |          | TSD_ADJ      |     |   |   |   |   |   |   |   | Thermal Adjust<br>00: 150 °C, 110 °C<br>01: 160 °C, 120 °C<br>10: 155 °C, 115 °C<br>11: 165 °C, 125 °C                                      |
|          |          | AMP_RES_MODE |     |   |   |   |   |   |   |   | AMP Resistor Selection Mode<br>0: Auto Set by 0x35 FDPEC_Control0[1:0]<br>FDPEC_GAIN<br>1: Manual Set by 0x35 FDPEC_Control0<br>[3] AMP_RES |
|          |          | LOW_PWR      |     |   |   |   |   |   |   |   | Low Power Mode<br>0: Normal<br>1: Low power                                                                                                 |
|          |          | FREQ_SEL     |     |   |   |   |   |   |   |   | SPK Output Frequency<br>0: 460 kHz<br>1: 560 kHz                                                                                            |
|          |          | SPK_DELAY    |     |   |   |   |   |   |   |   | SPK Output P / N Delay<br>0: 3.0 nsec<br>1: 0.2 nsec                                                                                        |
|          |          | SPK_FAST_OFF |     |   |   |   |   |   |   |   | SPK FAST OFF Function<br>0: FAST OFF Disable<br>1: FAST OFF Enable                                                                          |
|          |          | Default      | 0   | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0x0A                                                                                                                                        |

\*\* Don't use Address 0x40~0x8A

**PLL**

| Register | Function   | Name    | Bit |   |   |   |   |   |   |   | Description                    |
|----------|------------|---------|-----|---|---|---|---|---|---|---|--------------------------------|
|          |            |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                |
| 0x8B     | PLL_POST_N | POST_N  |     |   |   |   |   |   |   |   | POST_N[3:0] Post Divider Value |
|          |            | Default | 0   | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0x07                           |

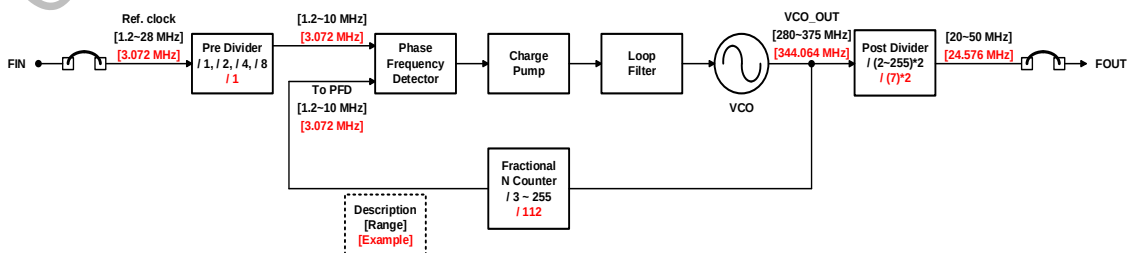
| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description                  |
|----------|----------|---------|-----|---|---|---|---|---|---|---|------------------------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                              |
| 0x8C     | PLL_N    | PLL_N   |     |   |   |   |   |   |   |   | N[7:0] Integer Divider Value |
|          |          | Default | 1   | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0xE0                         |

| Register | Function      | Name         | Bit |   |   |   |   |   |   |   | Description                                                                       |
|----------|---------------|--------------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------|
|          |               |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                   |
| 0x8D     | PLL_A_Setting | VCO_AMP_CTRL |     |   |   |   |   |   |   |   | VCO AMP Control                                                                   |
|          |               | CP_AMP_CTRL  |     |   |   |   |   |   |   |   | Charge Pump AMP Control                                                           |
|          |               | VCO_CTRL     |     |   |   |   |   |   |   |   | VCO Center Frequency<br>0000: 200 MHz<br>1011: 350 MHz (default)<br>1111: 450 MHz |
|          |               | Default      | 1   | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0x8B                                                                              |

| Register | Function | Name      | Bit |   |   |   |   |   |   |   | Description                                                                         |
|----------|----------|-----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------|
|          |          |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                     |
| 0x8E     | PLL_P,CP | LF_3RD_EN |     |   |   |   |   |   |   |   | Loop Filter order selection<br>0: 2 <sup>nd</sup> order<br>1: 3 <sup>rd</sup> order |
|          |          | LF_CTRL   |     |   |   |   |   |   |   |   | Loop Filter size selection<br>0: Low loop filter cap<br>1: Conventional             |
|          |          | PFD_SEL   |     |   |   |   |   |   |   |   | PFD_SEL[1:0] PFD delay time                                                         |
|          |          | PLL_P     |     |   |   |   |   |   |   |   | P[1:0] Pre-Divider Value                                                            |
|          |          | CP_CTRL   |     |   |   |   |   |   |   |   | CP_CTRL[1:0] Charge Pump Current                                                    |
|          |          | Default   | 0   | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0x10                                                                                |

**Recommended Setting for PLL**

| Input Frequency | Output Frequency | PLL_POST_N | PLL_N | PLL_A | PLL_P, CP |
|-----------------|------------------|------------|-------|-------|-----------|
| 1.536 MHz       | 24.576 MHz       | 0x06       | 0xC0  | 0x88  | 0x00      |
| 3.072 MHz       | 24.576 MHz       | 0x06       | 0x60  | 0x88  | 0x00      |
| 6.144 MHz       | 24.576 MHz       | 0x06       | 0x60  | 0x88  | 0x04      |
| 12.288 MHz      | 24.576 MHz       | 0x06       | 0x60  | 0x88  | 0x08      |



### Analog Test

| Register | Function | Name        | Bit |   |   |   |   |   |   |   | Description                                                                            |
|----------|----------|-------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------|
|          |          |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                        |
| 0x8F     | ANA_TEST | -           |     |   |   |   |   |   |   |   | Reserved                                                                               |
|          |          | BST_OCP_CLR |     |   |   |   |   |   |   |   | Select Boost OCP Latch Clear Signal<br>0: BST_EN or OCP_CLR<br>1: Global_EN or OCP_CLR |
|          |          | DIS_PVSS_SP |     |   |   |   |   |   |   |   | PVSS Short Protection Control<br>0: Enable<br>1: Disable                               |
|          |          | LOW_UVLO    |     |   |   |   |   |   |   |   | UVLO Level Control<br>0: 2.50V<br>1: 2.37V                                             |
|          |          | GM_CTRL     |     |   |   |   |   |   |   |   | OTA GM Control<br>00: 10uA/V<br>10: 20uA/V<br>11: 30uA/V                               |
|          |          | Default     | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                   |

### CrestLim

| Register | Function  | Name       | Bit |   |   |   |   |   |   |   | Description                                                                                                         |
|----------|-----------|------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------|
|          |           |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                     |
| 0x90     | CrestLim1 | CRSETLIM_1 |     |   |   |   |   |   |   |   | Limit integer value of Crest factor^2<br>(ex. crest factor = 4dB, crest factor^2 will be 2.51, CrestLim1=0000_0010) |
|          |           | Default    | 0   | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0x02                                                                                                                |

| Register | Function  | Name       | Bit |   |   |   |   |   |   |   | Description                                                                                                         |
|----------|-----------|------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------|
|          |           |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                     |
| 0x91     | CrestLim2 | CRSETLIM_2 |     |   |   |   |   |   |   |   | Limit decimal value of Crest factor^2<br>(ex. crest factor = 4dB, crest factor^2 will be 2.51, CrestLim2=1000_0010) |
|          |           | Default    | 1   | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0x82                                                                                                                |

### AMP and External Power Control

| Register | Function       | Name         | Bit |   |   |   |   |   |   |   | Description                                                                  |
|----------|----------------|--------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------|
|          |                |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                              |
| 0x92     | FDPEC Control1 | FLT_VDD_GAIN |     |   |   |   |   |   |   |   | Filtered VDD Gain Control<br>0000: FLT_VDD = 2.6 V<br>1111: FLT_VDD = 3.35 V |
|          |                | -            |     |   |   |   |   |   |   |   | Reserved                                                                     |
|          |                | DIS_FCHG     |     |   |   |   |   |   |   |   | Fast Charge<br>0: Enable<br>1: Disable                                       |
|          |                | -            |     |   |   |   |   |   |   |   | Reserved                                                                     |
|          |                | Default      | 1   | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0xB0                                                                         |

## Interrupt Control

| Register | Function   | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                         |
|----------|------------|---------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------|
|          |            |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                     |
| 0x93     | INTControl | -       |     |   |   |   |   |   |   |   | Reserved                                                                                            |
|          |            | SEL_INT |     |   |   |   |   |   |   |   | INT Operation Selection<br>0: INT clear automatically<br>1: INT clear can be set manually (0x93[1]) |
|          |            | CLR_INT |     |   |   |   |   |   |   |   | INT Clear<br>0: INT ready<br>1: INT clear (when INT clear bit "0x93[2] is H, can clear the INT)     |
|          |            | DIS_INT |     |   |   |   |   |   |   |   | INT Disable<br>0: Normal operation for INTN pin<br>1: High-Z for INT (INT skip mode)                |
|          |            | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                |

## BST Control\_1

| Register | Function      | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                         |
|----------|---------------|-----------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |               |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                     |
| 0x94     | BoostControl9 | SLOPE_OFF |     |   |   |   |   |   |   |   | Set Switching Off Slew<br>00: 6.7 nsec<br>01: 4.8 nsec<br>10: 2.6 nsec<br>11: 1.2 nsec                                                                                                                                              |
|          |               | SLOPE     |     |   |   |   |   |   |   |   | Set Switching Slew<br>00: 6.7 nsec<br>01: 4.8 nsec<br>10: 2.6 nsec<br>11: 1.2 nsec                                                                                                                                                  |
|          |               | -         |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                            |
|          |               | SET_RMP   |     |   |   |   |   |   |   |   | Set Ramp Compensation<br>000: 3.0 A / $\mu$ sec<br>001: 4.0 A / $\mu$ sec<br>010: 5.0 A / $\mu$ sec<br>011: 6.0A / $\mu$ sec<br>100: 7.0 A / $\mu$ sec<br>101: 8.0A / $\mu$ sec<br>110: 9.0A / $\mu$ sec<br>111: 10.0 A / $\mu$ sec |
|          |               | Default   | 0   | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0x54                                                                                                                                                                                                                                |

| Register | Function       | Name       | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                       |
|----------|----------------|------------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |                |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                   |
| 0x95     | BoostControl10 | HIGH_PGAIN |     |   |   |   |   |   |   |   | P-Gain Selection<br>1: Normal P-Gain<br>0: High P-Gain                                                                                                                                                                            |
|          |                | SET_OCL    |     |   |   |   |   |   |   |   | Set Overcurrent Limit<br>@ LOW_OCLN = 1<br>000: 2.6 A    001: 2.8 A<br>010: 3.0 A    011: 3.3 A<br>100: 3.6 A    101: 4.0 A<br>110: 4.5 A    111: 5.1 A<br>@ LOW_OCLN = 0<br>000: 1.7 A    001: 1.8 A<br>010: 2.0 A    011: 2.2 A |

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|  |  |          |   |   |   |   |   |   |   |                                                                                                                                                                                                                     |
|--|--|----------|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  |          |   |   |   |   |   |   |   | 100: 2.5 A    101: 2.7 A<br>110: 3.1 A    111: 3.5 A                                                                                                                                                                |
|  |  | SET_COMP |   |   |   |   |   |   |   | Set Loop Compensation<br>00XX : 30 pF I-gain<br>01XX : 60 pF I-gain<br>10XX : 90 pF I-gain<br>11XX : 120 pF I-gain<br>XX00: 0.5 MΩ P-gain<br>XX01: 0.375 MΩ P-gain<br>XX10: 0.25 MΩ P-gain<br>XX11: 0.125 MΩ P-gain |
|  |  | Default  | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0x4                                                                                                                                                                                                                 |

| Register | Function       | Name       | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                                                                                  |
|----------|----------------|------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |                |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                                                                              |
| 0x96     | BoostControl11 | SET_DT     |     |   |   |   |   |   |   |   | Set Driver On Deadtime<br>0000: 16.0 nsec<br>0001: 14.0 nsec<br>0010: 12.0 nsec<br>0011: 11.0 nsec<br>0100: 10.0 nsec<br>0101: 9.0 nsec<br>0110: 8.0 nsec<br>0111: 7.3 nsec<br>1000: 6.7 nsec<br>1001: 6.2 nsec<br>1010: 5.8 nsec<br>1011: 5.4 nsec<br>1100: 5.1 nsec<br>1101: 4.8 nsec<br>1110: 2.1 nsec<br>1111: 2.1 nsec  |
|          |                | SET_DT_OFF |     |   |   |   |   |   |   |   | Set Driver Off Deadtime<br>0000: 16.0 nsec<br>0001: 14.0 nsec<br>0010: 12.0 nsec<br>0011: 11.0 nsec<br>0100: 10.0 nsec<br>0101: 9.0 nsec<br>0110: 8.0 nsec<br>0111: 7.3 nsec<br>1000: 6.7 nsec<br>1001: 6.2 nsec<br>1010: 5.8 nsec<br>1011: 5.4 nsec<br>1100: 5.1 nsec<br>1101: 4.8 nsec<br>1110: 2.1 nsec<br>1111: 2.1 nsec |
|          |                | Default    | 0   | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0x44                                                                                                                                                                                                                                                                                                                         |

## SMA1857

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x97     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0x64        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x98     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 1   | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0x88        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x99     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x9A     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x9B     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0x64        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x9C     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 1   | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0xA4        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x9D     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

## SMA1857

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x9E     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0x9F     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

**PAD Control**

| Register | Function  | Name                | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|-----------|---------------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |           |                     | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0xA0     | PAD_CTRL0 | CLK_MON_SOURCE      |     |   |   |   |   |   |   |   | Clock Monitoring Source<br>00: SCK<br>01: PLL_OUT<br>10: SCK & PLL_LOCK<br>11: PLL_OUT & PLL_LOCK |
|          |           | -                   |     |   |   |   |   |   |   |   | Reserved                                                                                          |
|          |           | AUDIO_PD            |     |   |   |   |   |   |   |   | AUDIO Pull Down (SDI, SCK, LRCK)<br>0: Disable<br>1: Enable                                       |
|          |           | SDO_PU              |     |   |   |   |   |   |   |   | SDO Pull Up<br>0: Disable<br>1: Enable                                                            |
|          |           | INTN_PU             |     |   |   |   |   |   |   |   | INTN Pull Up<br>0: Disable<br>1: Enable                                                           |
|          |           | I <sup>2</sup> C_PU |     |   |   |   |   |   |   |   | I <sup>2</sup> C Pull Up (SDA, SCL)<br>0: Disable<br>1: Enable                                    |
|          |           | Default             | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                              |

| Register | Function  | Name    | Bit |   |   |   |   |   |   |   | Description                                                                     |
|----------|-----------|---------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------|
|          |           |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                 |
| 0xA1     | PAD_CTRL1 | INTN_DS |     |   |   |   |   |   |   |   | PAD Driver Strength Selection<br>0: 1.6 mA at 1.8 V IO<br>1: 3.2 mA at 1.8 V IO |
|          |           | SDO_DS  |     |   |   |   |   |   |   |   | PAD Driver Strength Selection<br>0: 1.6 mA at 1.8 V IO<br>1: 3.2 mA at 1.8 V IO |
|          |           | SDA_DS  |     |   |   |   |   |   |   |   | PAD Driver Strength Selection<br>0: 1.6 mA at 1.8 V IO<br>1: 3.2 mA at 1.8 V IO |
|          |           | LRCK_IE |     |   |   |   |   |   |   |   | PAD Input Enable Control<br>0: IE off<br>1: IE on                               |
|          |           | SCK_IE  |     |   |   |   |   |   |   |   | PAD Input Enable Control<br>0: IE off<br>1: IE on                               |
|          |           | SDI_IE  |     |   |   |   |   |   |   |   | PAD Input Enable Control<br>0: IE off<br>1: IE on                               |
|          |           | -       |     |   |   |   |   |   |   |   | Reserved                                                                        |
|          |           | Default | 0   | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0x3F                                                                            |

**Top Level Control\_1**

| Register | Function | Name        | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                              |
|----------|----------|-------------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                          |
| 0xA2     | TOP_MAN1 | -           |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                 |
|          |          | PLL_PD      |     |   |   |   |   |   |   |   | PLL Power Down<br>Before PLL turns on, set low for POWERUP bit (0x00[0]) to protect from unexpected status.<br>0: PLL operation<br>1: PLL power down                     |
|          |          | PLL_DIV     |     |   |   |   |   |   |   |   | PLL TEST Divider at SDO<br>00: PLL_OUT<br>01: PLL_OUT/2<br>10: PLL_OUT/4<br>11: PLL_OUT/8                                                                                |
|          |          | -           |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                 |
|          |          | LRSYNC_DIS  |     |   |   |   |   |   |   |   | LRSYNC_DIS<br>0: SYNC enable<br>1: SYNC disable                                                                                                                          |
|          |          | SDO_IO      |     |   |   |   |   |   |   |   | SDO Pad Output Control (I <sup>2</sup> S mode)<br>0: High-Z at LRCK H<br>(data(SDO_OUT0) valid at LRCK = L)<br>1: High-Z at LRCK L<br>(data(SDO_OUT1) valid at LRCK = H) |
|          |          | SDO_OUTPUT2 |     |   |   |   |   |   |   |   | SDO Output Control (I <sup>2</sup> S mode)<br>0: One SDO output per channel<br>(High-Z and SDO_OUT0/1)<br>1: Two SDO outputs per channel<br>(SDO_OUT0 and SDO_OUT1)      |
|          |          | Default     | 0   | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0x4C                                                                                                                                                                     |

| Register | Function | Name        | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                             |
|----------|----------|-------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                         |
| 0xA3     | TOP_MAN2 | MON_OSC_PLL |     |   |   |   |   |   |   |   | Monitoring OSC and PLL<br>00: Data output at SDO<br>(Data are selected by 0x09[5:0])<br>01: Monitoring PLL at SDO<br>10: Reserved<br>11: Monitoring Internal OSC at SDO |
|          |          | -           |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                |
|          |          | SDO_OUPUT1  |     |   |   |   |   |   |   |   | SDO Output<br>0: Logic output<br>1: High-Z                                                                                                                              |
|          |          | SDO_OUTPUT3 |     |   |   |   |   |   |   |   | SDO Output Control (I <sup>2</sup> S mode)<br>0: SDO Output set by<br>(SDO_OUTPUT2(0xA2[0]))<br>1: Two SDO outputs per channel (24 kHz)<br>(SDO_OUT0 and SDO_OUT1)      |
|          |          | CLOCK_MON   |     |   |   |   |   |   |   |   | 0: Monitoring<br>1: Not monitoring                                                                                                                                      |
|          |          | OSC_PD      |     |   |   |   |   |   |   |   | Internal OSC<br>0: Internal OSC Enable<br>1: Power down                                                                                                                 |
|          |          | Default     | 0   | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0x28                                                                                                                                                                    |

| Register | Function | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                                                |
|----------|----------|-----------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------|
|          |          |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                            |
| 0xA4     | TOP_MAN3 | INTERFACE |     |   |   |   |   |   |   |   | Interface Format<br>000: Reserved<br>001: LJ<br>010: I <sup>2</sup> S<br>011: Reserved<br>100: TDM<br>101 to 111: Reserved |
|          |          | SCK_RATE  |     |   |   |   |   |   |   |   | Sample Rate for I <sup>2</sup> S<br>00, 01: 64 fs<br>10, 11: 32 fs                                                         |
|          |          | DATA_W    |     |   |   |   |   |   |   |   | DATA Width for I <sup>2</sup> S<br>00: 24-bit<br>01/10: don't use<br>11: 16-bit                                            |
|          |          | LRCK_POL  |     |   |   |   |   |   |   |   | 0: L valid<br>1: H valid                                                                                                   |
|          |          | Default   | 0   | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0x40                                                                                                                       |

### TDM Control

| Register | Function | Name             | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                            |
|----------|----------|------------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                  | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                        |
| 0xA5     | TDM1     | -                |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                               |
|          |          | TDM_STEREO       |     |   |   |   |   |   |   |   | Number of TDM Output Control<br>0: SDO_OUT0 only<br>1: SDO_OUT0 and SDO_OUT1                                                                                           |
|          |          | TDM_SLOT1_POS_RX |     |   |   |   |   |   |   |   | TDM Input0 Slot Position (fs = 48 kHz, 16-bit / 32-bit, and 4-slot / 8-slot are valid)<br>000: 0<br>001: 1<br>010: 2<br>011: 3<br>100: 4<br>101: 5<br>110: 6<br>111: 7 |
|          |          | TDM_SLOT2_POS_RX |     |   |   |   |   |   |   |   | TDM Input1 Slot Position (fs = 48 kHz, 16-bit / 32-bit, and 4-slot / 8-slot are valid)<br>000: 0<br>001: 1<br>010: 2<br>011: 3<br>100: 4<br>101: 5<br>110: 6<br>111: 7 |
|          |          | Default          | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x01                                                                                                                                                                   |

| Register | Function | Name       | Bit |   |   |   |   |   |   |   | Description                               |
|----------|----------|------------|-----|---|---|---|---|---|---|---|-------------------------------------------|
|          |          |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                           |
| 0xA6     | TDM2     | TDM_DL     |     |   |   |   |   |   |   |   | TDM Data Length<br>0: 16-bit<br>1: 32-bit |
|          |          | TDM_N_SLOT |     |   |   |   |   |   |   |   | TDM Number of Slot<br>Value : n-Slot      |

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|  |  |                  |   |   |   |   |   |   |   |                                                                                                                                                                            |
|--|--|------------------|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  |                  |   |   |   |   |   |   |   | 0: 4<br>1: 8                                                                                                                                                               |
|  |  | TDM_SLOT_POS_TX  |   |   |   |   |   |   |   | TDM Output (SDO_OUT0) Slot Position<br>000: 0<br>001: 1<br>010: 2<br>011: 3<br>100: 4<br>101: 5<br>110: 6<br>111: 7                                                        |
|  |  | TDM_SLOT2_POS_TX |   |   |   |   |   |   |   | TDM Output (SDO_OUT1) Slot Position<br>Valid only when Number of TDM output control is "1"<br>000: 0<br>001: 1<br>010: 2<br>011: 3<br>100: 4<br>101: 5<br>110: 6<br>111: 7 |
|  |  | Default          | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1<br>0x41                                                                                                                                                                  |

### Top Level Control\_2

| Register | Function | Name             | Bit |   |   |   |   |   |   |   | Description                                                                                                                                           |
|----------|----------|------------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                  | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                       |
| 0xA7     | CLK_MON  | CLK_MON_TIME_SEL |     |   |   |   |   |   |   |   | Clock Monitoring Time Selection<br>00: 80 $\mu$ sec<br>01: 40 $\mu$ sec<br>10: 20 $\mu$ sec<br>11: 10 $\mu$ sec                                       |
|          |          | DITHER           |     |   |   |   |   |   |   |   | Dither Gen. for Modulator<br>0: Off<br>1: On                                                                                                          |
|          |          | EN_A_TV          |     |   |   |   |   |   |   |   | Additional Tone Volume Enable<br>0: Normal tone volume<br>1: Additional tone volume<br>(if EN_A_TV = 1, Tone vol can be changed from -60 dB ~ -96 dB) |
|          |          | TEST_LIMITER     |     |   |   |   |   |   |   |   | TEST of Limiter Operating Range<br>0: Disable<br>1: Enable                                                                                            |
|          |          | -                |     |   |   |   |   |   |   |   | Reserved                                                                                                                                              |
|          |          | Default          | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                                                  |

**BST CONTROL\_2**

| Register | Function      | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                           |
|----------|---------------|---------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |               |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                       |
| 0xA8     | BoostControl1 | -       |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                                                              |
|          |               | MIN_V   |     |   |   |   |   |   |   |   | Set Skip Mode Control Range<br>Pulse Skipping mode control at<br>VBST < VBAT + minV<br>minV = MIN_V / 64 * Boost Gain<br>Ex) 01100 = 1.77V at FDPEC_GAIN = 10<br>** Boost Gain =<br>6.8 at FDPEC_GAIN = 00 or 01<br>9.4 at FDPEC_GAIN = 10<br>11.2 at FDPEC_GAIN = 11 |
|          |               | Default | 0   | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0x0C                                                                                                                                                                                                                                                                  |

| Register | Function      | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                  |
|----------|---------------|-----------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |               |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                              |
| 0xA9     | BoostControl2 | SOFT_CLK  |     |   |   |   |   |   |   |   | Set Clock Speed for Soft Start<br>Boost Reference is changed at every<br>(1 + SOFT_CLK) / BST_FREQ                                                                                                                           |
|          |               | HEAD_ROOM |     |   |   |   |   |   |   |   | Set Head Room Voltage<br>Head Room Voltage = HEAD_ROOM / 64<br>* Boost Gain<br>Ex) 00100 = 0.589V at FDPEC_GAIN = 10<br>** Boost Gain =<br>6.8 at FDPEC_GAIN = 00 or 01<br>9.4 at FDPEC_GAIN = 10<br>11.2 at FDPEC_GAIN = 11 |
|          |               | Default   | 0   | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0x24                                                                                                                                                                                                                         |

| Register | Function      | Name      | Bit |   |   |   |   |   |   |   | Description                                                            |
|----------|---------------|-----------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------|
|          |               |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                        |
| 0xAA     | BoostControl3 | -         |     |   |   |   |   |   |   |   | Reserved                                                               |
|          |               | HOLD_TIME |     |   |   |   |   |   |   |   | Set Hold Time<br>Hold Time = HOLD_TIME * 1/48K*128<br>000000: Reserved |
|          |               | Default   | 0   | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0x10                                                                   |

| Register | Function      | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                         |
|----------|---------------|-----------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |               |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                     |
| 0xAB     | BoostControl4 | -         |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                                                                                                            |
|          |               | BOOST_MAX |     |   |   |   |   |   |   |   | Set Maximum Boost Voltage<br>00000: Reserved<br>Max. Boost Voltage =<br>BOOST_MAX / 16 * Boost Gain<br>Ex) 10001 = 10.0V<br>** Boost Gain = at FDPEC_GAIN = 10<br>6.8 at FDPEC_GAIN = 00 or 01<br>9.4 at FDPEC_GAIN = 10<br>11.2 at FDPEC_GAIN = 11 |
|          |               | Default   | 0   | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0x13                                                                                                                                                                                                                                                |

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| Register | Function      | Name       | Bit |   |   |   |   |   |   |   | Description                                                                   |
|----------|---------------|------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------------------|
|          |               |            | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                               |
| 0xAC     | BoostControl5 | -          |     |   |   |   |   |   |   |   | Reserved                                                                      |
|          |               | BOOST_MODE |     |   |   |   |   |   |   |   | Boost Mode Control<br>00: Class-H<br>01: Forced on<br>10: Off<br>11: Reserved |
|          |               | SKIP_PULSE |     |   |   |   |   |   |   |   | Set Skip Pulse number without switching in pulse skipping mode.               |
|          |               | Default    | 0   | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0x10                                                                          |

| Register | Function      | Name         | Bit |   |   |   |   |   |   |   | Description                                                       |
|----------|---------------|--------------|-----|---|---|---|---|---|---|---|-------------------------------------------------------------------|
|          |               |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                   |
| 0xAD     | BoostControl6 | RELEASE_TIME |     |   |   |   |   |   |   |   | Set Release Time<br>Release Time =<br>(RELEASE_TIME + 1) * 1/192k |
|          |               | Default      | 0   | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0x10                                                              |

| Register | Function      | Name         | Bit |   |   |   |   |   |   |   | Description                                                                                                                                         |
|----------|---------------|--------------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------|
|          |               |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                     |
| 0xAE     | BoostControl7 | BST_ON_DELAY |     |   |   |   |   |   |   |   | Set BST_ON Delay<br>Delay = (1 + BST_ON_DELAY) /<br>BST_FREQ                                                                                        |
|          |               | BST_FREQ     |     |   |   |   |   |   |   |   | Set Boost Frequency<br>000: 1.4 MHz<br>001: 1.5 MHz<br>010: 1.8 MHz<br>011: 2.0 MHz<br>100: 2.2 MHz<br>101: 2.5 MHz<br>110: 2.7 MHz<br>111: 3.1 MHz |
|          |               | MIN_DUTY     |     |   |   |   |   |   |   |   | Set Minimum On-Time<br>00: 40 nsec<br>01: 80 nsec<br>10: 120 nsec<br>11: 160 nsec                                                                   |
|          |               | Default      | 1   | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0xCD                                                                                                                                                |

| Register | Function | Name   | Bit |   |   |   |   |   |   |   | Description                                                                                       |
|----------|----------|--------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------|
|          |          |        | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                   |
| 0xAF     | LPF      | COEF_A |     |   |   |   |   |   |   |   | Filter Tuning Coefficient<br>COEF_A<br>00: 0<br>01: 1/2^4<br>10: 1/2^3<br>11: 1/2^2               |
|          |          | COEF_B |     |   |   |   |   |   |   |   | Filter Tuning Coefficient<br>COEF_B<br>000: 0<br>001: 1/2^6<br>010: 1/2^5<br>011: 1/2^4<br>100: 0 |

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|  |  |         |   |   |   |   |   |   |   |   |   |                                                                                                                                                                                   |
|--|--|---------|---|---|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  |         |   |   |   |   |   |   |   |   |   | 101: -1/2 <sup>6</sup><br>110: -1/2 <sup>5</sup><br>111: -1/2 <sup>4</sup>                                                                                                        |
|  |  | COEF_C  |   |   |   |   |   |   |   |   |   | Filter Tuning Coefficient<br>COEF_C<br>000: 0<br>001: 1/2 <sup>8</sup><br>010: 1/2 <sup>7</sup><br>011: 0<br>100: 0<br>101: -1/2 <sup>8</sup><br>110: -1/2 <sup>7</sup><br>111: 0 |
|  |  | Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x41                                                                                                                                                                              |

LPF Tuning Table

| COEF_A | COEF_B | COEF_C | Cut-off Frequency (Fc) [Hz] |
|--------|--------|--------|-----------------------------|
| 01     | 111    | 001    | 59.3                        |
| 01     | 111    | 010    | 119.3                       |
| 01     | 110    | 110    | 361.3                       |
| 01     | 110    | 101    | 422.6                       |
| 01     | 110    | 000    | 484.0                       |
| 01     | 110    | 001    | 545.3                       |
| 01     | 101    | 110    | 607.3                       |
| 01     | 101    | 101    | 669.3                       |
| 01     | 101    | 000    | 732.0                       |
| 01     | 101    | 001    | 794.6                       |
| 01     | 000    | 110    | 857.3                       |
| 01     | 000    | 101    | 920.6                       |
| 01     | 000    | 000    | 984.0                       |
| 01     | 000    | 001    | 1048.0                      |
| 01     | 000    | 010    | 1112.0                      |
| 01     | 001    | 101    | 1176.0                      |
| 01     | 001    | 000    | 1240.6                      |
| 01     | 001    | 001    | 1305.3                      |
| 01     | 010    | 110    | 1370.6                      |
| 01     | 010    | 101    | 1436.0                      |
| 01     | 010    | 000    | 1502.0                      |
| 01     | 010    | 001    | 1568.0                      |
| 01     | 010    | 010    | 1634.0                      |
| 10     | 101    | 101    | 1700.6                      |
| 10     | 101    | 000    | 1767.3                      |
| 10     | 101    | 001    | 1834.6                      |
| 10     | 000    | 110    | 1902.6                      |
| 10     | 000    | 101    | 1970.0                      |
| 10     | 000    | 000    | 2038.6                      |
| 10     | 000    | 001    | 2106.6                      |
| 10     | 000    | 010    | 2176.0                      |
| 10     | 001    | 101    | 2244.6                      |
| 10     | 001    | 000    | 2314.6                      |

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|    |     |     |        |
|----|-----|-----|--------|
| 10 | 001 | 001 | 2384.0 |
| 10 | 010 | 110 | 2454.6 |
| 10 | 010 | 101 | 2525.3 |
| 10 | 010 | 000 | 2596.0 |
| 10 | 010 | 001 | 2667.3 |
| 10 | 010 | 010 | 2738.6 |
| 10 | 011 | 110 | 3029.3 |
| 11 | 111 | 101 | 3102.6 |
| 11 | 111 | 000 | 3176.6 |
| 10 | 011 | 001 | 3250.6 |
| 10 | 011 | 010 | 3325.3 |
| 11 | 110 | 110 | 3628.0 |
| 11 | 110 | 101 | 3704.6 |
| 11 | 110 | 000 | 3782.0 |
| 11 | 110 | 001 | 3859.3 |
| 11 | 101 | 110 | 3937.3 |
| 11 | 101 | 101 | 4016.0 |
| 11 | 101 | 000 | 4095.3 |
| 11 | 101 | 001 | 4174.6 |
| 11 | 000 | 110 | 4254.6 |
| 11 | 000 | 101 | 4334.6 |
| 11 | 000 | 000 | 4415.3 |
| 11 | 000 | 001 | 4496.6 |
| 11 | 000 | 010 | 4578.6 |
| 11 | 001 | 101 | 4660.6 |
| 11 | 001 | 000 | 4744.0 |
| 11 | 001 | 001 | 4826.6 |
| 11 | 010 | 110 | 4910.6 |
| 11 | 010 | 101 | 4995.3 |
| 11 | 010 | 000 | 5080.0 |
| 11 | 010 | 001 | 5165.3 |
| 11 | 010 | 010 | 5251.3 |
| 11 | 011 | 110 | 5600.6 |
| 11 | 011 | 101 | 5690.0 |
| 11 | 011 | 000 | 5779.3 |
| 11 | 011 | 001 | 5869.3 |
| 11 | 011 | 010 | 5960.0 |

**POWER METER2**

| Register | Function | Name           | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                    |
|----------|----------|----------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                |
| 0xB0     | RMS_TC1  | PEAK_THR       |     |   |   |   |   |   |   |   | Peak Detection Threshold<br>(monitoring Peak flag 0xFA[1])<br>0: over -12 dB , 1: over -9 dB                                                                   |
|          |          | DATA_FORMAT    |     |   |   |   |   |   |   |   | 0: Unsinged data at SDO<br>1: Singed data at SDO                                                                                                               |
|          |          | -              |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                       |
|          |          | RMS_TIME_CONST |     |   |   |   |   |   |   |   | RMS Time const[10:8] : RMS time constant<br>MSB<br>*Time = 5.44 sec / X<br>000_0000_0000: Don't use<br>000_0000_0001: 5.4 sec<br>~<br>111_11111_1111: 2.6 msec |
|          |          | Default        | 0   | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0x07                                                                                                                                                           |

| Register | Function | Name            | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                    |
|----------|----------|-----------------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                |
| 0xB1     | RMS_TC2  | RMS_TIME_CONST2 |     |   |   |   |   |   |   |   | RMS Time Const [7:0] : RMS time constant<br>LSB<br>*Time = 5.44 sec / X<br>000_0000_0000: Don't use<br>000_0000_0001: 5.4 sec<br>~<br>111_11111_1111: 2.6 msec |
|          |          | Default         | 1   | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0xFF                                                                                                                                                           |

| Register | Function | Name            | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                      |
|----------|----------|-----------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                  |
| 0xB2     | AVG_TC1  | -               |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                         |
|          |          | AVG_TIME_CONST1 |     |   |   |   |   |   |   |   | AVGTime Const[10:8]: Average time<br>constant MSB<br>*Time = 5.44 sec / X<br>000_0000_0000: Don't use<br>000_0000_0001: 5.4 sec<br>~<br>111_11111_1111: 2.6 msec |
|          |          | Default         | 0   | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0x07                                                                                                                                                             |

| Register | Function | Name            | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                      |
|----------|----------|-----------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                  |
| 0xB3     | AVG_TC2  | AVG_TIME_CONST2 |     |   |   |   |   |   |   |   | AVGTime Const[7:0] : Average time<br>constant LSB<br>*Time = 5.44 sec / X<br>000_0000_0000: Don't use<br>000_0000_0001: 5.4 sec<br>~<br>111_11111_1111: 2.6 msec |
|          |          | Default         | 1   | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0xFF                                                                                                                                                             |

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| Register | Function  | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                                                  |
|----------|-----------|-----------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------|
|          |           |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                              |
| 0xB4     | PR_VALUE1 | PR_VALUE1 |     |   |   |   |   |   |   |   | PR Value[15:8] :Wanted Limit Value of RMS^2<br>See the calculation table.<br>Default : 0.5 W limit at 4 V supply, 8 $\Omega$ |
|          |           | Default   | 1   | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0xE0                                                                                                                         |

| Register | Function  | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                                                  |
|----------|-----------|-----------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------|
|          |           |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                              |
| 0xB5     | PR_VALUE2 | PR_VALUE2 |     |   |   |   |   |   |   |   | PR Value[7:0] : Wanted Limit Value of RMS^2<br>See the calculation table.<br>Default : 0.5 W limit at 4 V supply, 8 $\Omega$ |
|          |           | Default   | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                         |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0xB6     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |
| 0xB7     | -        | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved    |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00        |

### SPK Noise Gate

| Register | Function     | Name   | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                   |
|----------|--------------|--------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |              |        | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                               |
| 0xB8     | SPK_NG_CTRL1 | -      |     |   |   |   |   |   |   |   | Reserved                                                                                                                                                      |
|          |              | NG_EN  |     |   |   |   |   |   |   |   | SPK noise gate function enable<br>0: disable<br>1: enable                                                                                                     |
|          |              | NG_VTH |     |   |   |   |   |   |   |   | SPK Noise Gate Threshold<br>000: -85dBFS<br>001: -90dBFS<br>010: -95dBFS<br>011: -100dBFS<br>100: -105dBFS<br>101: -110dBFS<br>110: -115dBFS<br>111: -120dBFS |
|          |              | NG_ATK |     |   |   |   |   |   |   |   | Noise Gate Attack Time<br>000: 5msec<br>001:10msec<br>010:25msec<br>011:50msec<br>100:100msec<br>101:200msec<br>110:500msec                                   |

# SMA1857

|  |  |         |   |   |   |   |   |   |   |   |          |
|--|--|---------|---|---|---|---|---|---|---|---|----------|
|  |  |         |   |   |   |   |   |   |   |   | 111:1sec |
|  |  | Default | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0x22     |

| Register | Function     | Name              | Bit |   |   |   |   |   |   |   | Description                                                                                                  |
|----------|--------------|-------------------|-----|---|---|---|---|---|---|---|--------------------------------------------------------------------------------------------------------------|
|          |              |                   | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                              |
| 0xB9     | SPK_NG_CTRL2 | ANA_SETUP_DLY_EN  |     |   |   |   |   |   |   |   | Analog setup delay enable<br>0: Disable<br>1: Enable                                                         |
|          |              | CLK_FAULT_MODE    |     |   |   |   |   |   |   |   | Clock Fault mode selection<br>0: Initial High before clock input<br>0: Initial Low before clock input        |
|          |              | NG_ON_FALLING_INT |     |   |   |   |   |   |   |   | Noise Gate Falling Manual interrupt Mode enable<br>0: Disable<br>1: Enable                                   |
|          |              | NG_ON_RISING_INT  |     |   |   |   |   |   |   |   | Noise Gate Rising Manual interrupt Mode enable<br>0: Disable<br>1: Enable                                    |
|          |              | ENV_RST_TRIM      |     |   |   |   |   |   |   |   | 0: Nrst low when Clock Fault<br>1: AP_PD high when Clock Fault                                               |
|          |              | INT_I2C_LATCH_EN  |     |   |   |   |   |   |   |   | 0: Disable<br>1: Enable (Enable only when 0x93[2] = 1)                                                       |
|          |              | NG_SOURCE_SEL     |     |   |   |   |   |   |   |   | Noise Gate Source Selection<br>00: Left<br>01: Right<br>10: Left   Right @stereo<br>11: Left & Right @stereo |
|          |              | Default           | 1   | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0x87                                                                                                         |

## DGC

| Register | Function | Name            | Bit |   |   |   |   |   |   |   | Description                                                                                                                             |
|----------|----------|-----------------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                         |
| 0xBA     | DGC_1    | ATTACK_DGC      |     |   |   |   |   |   |   |   | Attack_time<br>000: 20msec<br>001: 40msec<br>010: 60msec<br>011: 80msec<br>100: 100msec<br>101: 120msec<br>110: 140msec<br>111: 160msec |
|          |          | TIMEOUT_DGC     |     |   |   |   |   |   |   |   | Timeout<br>00: 80msec<br>01: 100msec<br>10: 200msec<br>11: 250msec                                                                      |
|          |          | DGC_REF_TEST_EN |     |   |   |   |   |   |   |   | Reference Signal Selection enable<br>0:Default<br>1:Enable                                                                              |
|          |          | ZCR_EN          |     |   |   |   |   |   |   |   | ZCR_EN<br>0: Disable<br>1: Enable                                                                                                       |
|          |          | DGC_EN          |     |   |   |   |   |   |   |   | DGC_EN<br>0: Disable<br>1: Enable                                                                                                       |
|          |          | Default         | 1   | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0x82                                                                                                                                    |

| Register | Function | Name            | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|----------|-----------------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |                 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 0xBB     | DGC_2    | DGC_THR         |     |   |   |   |   |   |   |   | DGC Threshold<br>When Test Mode disable<br>DGC_TEST_EN(0xBB[0] = 1'b0)<br>000000: DGC off<br>0000001: 0.003906fs (-48dB)<br>0000010: 0.007813fs (-42dB)<br>...<br>1110000: 0.4375fs (-7dB)<br>...<br>1111111: 0.496094fs (-6dB)<br>0.003906fs with every step<br><br>When Test Mode enable<br>DGC_TEST_EN(0xBB[0] = 1'b1)<br>0000000: DGC off<br>0000001 ~ 0011111: Reserved<br>0100000: 0.0000305184fs (-90dB)<br>...<br>1110000: 0.0001068115 fs (-79dB)<br>...<br>1111111: 0.0001211166 fs (-78dB)<br>0.0000009537fs with every step |
|          |          | DGC_THR_TEST_EN |     |   |   |   |   |   |   |   | Test Mode enable<br>0: Default<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|          |          | Default         | 0   | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0x41                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description                                                                                                                                                                                                    |
|----------|----------|---------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                                                                                                                |
| 0xBC     | DGC_3    | DGC_DLY |     |   |   |   |   |   |   |   | Dynamic Gain Control (DGC) Delay Set<br>0000_0000: 0 ns<br>0000_0001: 40 ns<br>.....<br>1111_1111: 10, 200 ns<br>*Delay can be controlled by system clock ratio.<br>*DGC on / off can be controlled by 0xB7[0] |
|          |          | Default | 1   | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0x94                                                                                                                                                                                                           |

### MCBS(Multi Chip Balancing Solution)

| Register | Function    | Name      | Bit |   |   |   |   |   |   |   | Description                                                                                              |
|----------|-------------|-----------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------|
|          |             |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                          |
| 0xBD     | MCBS_CTRL_1 | -         |     |   |   |   |   |   |   |   | Reserved                                                                                                 |
|          |             | MCBS_MODE |     |   |   |   |   |   |   |   | MCBS MODE<br>0: Tracking by Limiter Threshold<br>1: Tracking by Limiter Gain Value                       |
|          |             | MCBS_EN   |     |   |   |   |   |   |   |   | MCBS function enable<br>0: disable<br>1: enable                                                          |
|          |             | MCBS_DEV1 |     |   |   |   |   |   |   |   | MCBS Device1 Slot Select<br>0000: disable<br>0001: Time Slot 0<br>0010: Time Slot 1<br>0011: Time Slot 2 |

# SMA1857

|  |  |         |   |   |   |   |   |   |   |                                                                                                                               |
|--|--|---------|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------------------------------|
|  |  |         |   |   |   |   |   |   |   | 0100: Time Slot 3<br>0101: Time Slot 4<br>0110: Time Slot 5<br>0111: Time Slot 6<br>1000: Time Slot 7<br>1001 ~ 1111: disable |
|  |  | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                                                                          |

[illegible]

## Status Register Read Only

[illegible][illegible][illegible]

# SMA1857

| Register | Function  | Name         | Bit |   |   |   |   |   |   |   | Description                                                                     |
|----------|-----------|--------------|-----|---|---|---|---|---|---|---|---------------------------------------------------------------------------------|
|          |           |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                 |
| 0xF9     | Status_T2 | TEMP_MON_LSB |     |   |   |   |   |   |   |   | TEMP_MON_OUT[7:0]<br>*To get the exact temperature data, run "Read 0xF7" first. |
|          |           | Default      | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                            |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description                                                                       |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                   |
| 0xFA     | Status1  | OT1_OK  |     |   |   |   |   |   |   |   | Low Threshold<br>0: Over-temperature situation in chip<br>1: Chip-temperature OK  |
|          |          | OT2_OK  |     |   |   |   |   |   |   |   | High Threshold<br>0: Over-temperature situation in chip<br>1: Chip-temperature OK |
|          |          | UVLO    |     |   |   |   |   |   |   |   | UVLO<br>0: Normal<br>1: under voltage situation                                   |
|          |          | BST_OS  |     |   |   |   |   |   |   |   | Over Voltage Protection of BST<br>0: Normal<br>1: Over voltage protection         |
|          |          | POWER_F |     |   |   |   |   |   |   |   | Power Flag<br>0: Normal<br>1: Power Over Limit                                    |
|          |          | -       |     |   |   |   |   |   |   |   | Reserved                                                                          |
|          |          | NG_ON   |     |   |   |   |   |   |   |   | NG_ON monitoring<br>0: Normal Operation<br>1: Noise gated Operation               |
|          |          | Default | 1   | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0xC0                                                                              |

| Register | Function | Name      | Bit |   |   |   |   |   |   |   | Description                                                                |
|----------|----------|-----------|-----|---|---|---|---|---|---|---|----------------------------------------------------------------------------|
|          |          |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                            |
| 0xFB     | Status2  | SCAN_CHK  |     |   |   |   |   |   |   |   | Scan Check<br>0: Normal<br>1: Scan                                         |
|          |          | -         |     |   |   |   |   |   |   |   | Reserved                                                                   |
|          |          | OCP_SPK   |     |   |   |   |   |   |   |   | 0: Output-stage OK<br>1: Overcurrent situation in SPK output-stage         |
|          |          | OCP_BST   |     |   |   |   |   |   |   |   | 0: Output-stage OK<br>1: Overcurrent situation in SPK_BST output-stage     |
|          |          | BOP_STATE |     |   |   |   |   |   |   |   | BOP status                                                                 |
|          |          | CLOCK_MON |     |   |   |   |   |   |   |   | Clock Fault Monitoring<br>0: Normal operation<br>1: Fault (no clock input) |
|          |          | Default   | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                       |

| Register | Function | Name         | Bit |   |   |   |   |   |   |   | Description                                                                  |
|----------|----------|--------------|-----|---|---|---|---|---|---|---|------------------------------------------------------------------------------|
|          |          |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                              |
| 0xFC     | Status3  | -            |     |   |   |   |   |   |   |   | Reserved                                                                     |
|          |          | VBAT_MON_MSB |     |   |   |   |   |   |   |   | VBAT_MON_OUT[11:8]<br>*To get the exact battery data, run "Read 0xF5" first. |

## SMA1857

|  |  |         |   |   |   |   |   |   |   |   |      |
|--|--|---------|---|---|---|---|---|---|---|---|------|
|  |  | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
|--|--|---------|---|---|---|---|---|---|---|---|------|

| Register | Function | Name         | Bit |   |   |   |   |   |   |   | Description                                                                 |
|----------|----------|--------------|-----|---|---|---|---|---|---|---|-----------------------------------------------------------------------------|
|          |          |              | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                                             |
| 0xFD     | Status4  | VBAT_MON_LSB |     |   |   |   |   |   |   |   | VBAT_MON_OUT[7:0]<br>*To get the exact battery data, run "Read 0xF5" first. |
|          |          | Default      | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00                                                                        |

| Register | Function | Name    | Bit |   |   |   |   |   |   |   | Description                                   |
|----------|----------|---------|-----|---|---|---|---|---|---|---|-----------------------------------------------|
|          |          |         | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                               |
| 0xFE     | Status5  | -       |     |   |   |   |   |   |   |   | Reserved                                      |
|          |          | INTN    |     |   |   |   |   |   |   |   | INTN status<br>0: interrupt case<br>1: normal |
|          |          | INT     |     |   |   |   |   |   |   |   | INT status<br>0: normal<br>1: interrupt case  |
|          |          | Default | 0   | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0x02                                          |

| Register | Function     | Name      | Bit |   |   |   |   |   |   |   | Description                                            |
|----------|--------------|-----------|-----|---|---|---|---|---|---|---|--------------------------------------------------------|
|          |              |           | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                        |
| 0xFF     | Device_Index | DEVICE_ID |     |   |   |   |   |   |   |   | Device ID<br>00011: SMA1857                            |
|          |              | REV_NUM   |     |   |   |   |   |   |   |   | Revision Number<br>000: MVT0<br>001: MVT1<br>010: MVT2 |
|          |              | Default   | 0   | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0x1A                                                   |

## Package Information

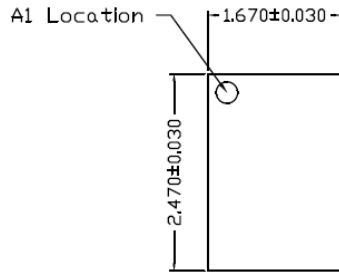
| Orderable Device | Package Type | Pins | Temp. Range      | Eco Plan       |
|------------------|--------------|------|------------------|----------------|
| SMA1857-W        | WLCSP        | 24   | -25 °C to +85 °C | Pb-Free / RoHS |

Dimensions are in millimeters, unless otherwise specified.

### WLCSP

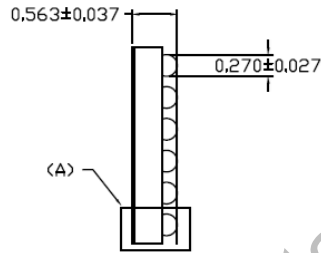
#### NOTES:

1. ALL DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

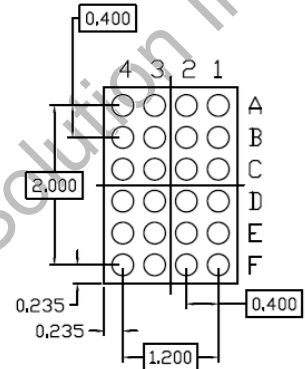


BSP SIDE VIEW

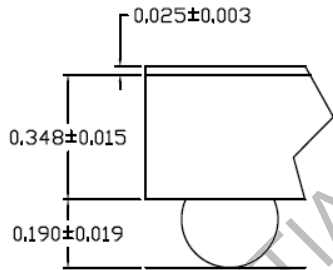
WAFER Notch zone direction : 6 o'clock



SIDE VIEW



BALL SIDE VIEW



(A) x4 Zoom CW 90 Degree Rotated

| Item                 | Unit | Mln   | Normal | Max   |
|----------------------|------|-------|--------|-------|
| PKG Body Dimension X | mm   | 1.640 | 1.670  | 1.700 |
| PKG Body Dimension Y | mm   | 2.440 | 2.470  | 2.500 |
| PKG Total Height     | mm   | 0.526 | 0.563  | 0.600 |
| DIE Thickness        | mm   | 0.333 | 0.348  | 0.363 |
| Backside Coating     | mm   | 0.022 | 0.025  | 0.028 |
| Ball Height          | mm   | 0.171 | 0.190  | 0.209 |
| Ball Dimension       | mm   | 0.243 | 0.270  | 0.297 |
| Ball Pitch X         | mm   | -     | 0.400  | -     |
| Ball Pitch Y         | mm   | -     | 0.400  | -     |
| Total Ball Count     | ea   | -     | 24     | -     |

## ***Revision History***

[illegible]

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