

F1DR8761C

Datasheet

MODEL : F1DR8761C
DATE : MAY 21, 2024
REVISION : 0.1

Issued by

Checked by

Approved by



2024.05.21

<http://www.f1-media.com>

9F, Keumkang Hightech II, 159, Sagimakgol-ro, Jungwon-gu,
Seongnam-si, Gyeonggi-do, Korea 13202

Revision History

Revision	Date	Change Descriptions	Issued by
0.1	2024.05.21	Initial Release	H.S MOON

List of Contents

1. General	4
1.1. Overview	4
1.2. Feature	5
1.3. Application	5
2. Pin Definition	6
2.1. Pinout Diagram	6
2.2. Device Terminal Descriptions	7
3. General specification	8
3.1. Electrical Characteristics	8
3.1.1. Absolute Maximum Ratings	8
3.1.2. Recommended Operating Conditions	8
3.1.3. Power Consumption	8
4. Bluetooth RF Specifications	9
4.1. BR + EDR RF specification	9
4.1.1. BR + EDR Receiver	9
4.1.2. BR + EDR Transmitter	9
4.1.3. LE Receiver	9
4.1.4. LE Transmitter	9
5. Interface	10
5.1. UART Interface	10
5.2. Digital Audio Interface	10
5.2.1. PCM/I2S	10
5.3. LED	12
6. Reference Schematic	13
7. Dimension	14
7.1. Module Dimensions	14
7.2. Recommended Footprint	15
8. Reflow Temperature Profile	16
9. Module Placement Rule	17

1. General

1.1.Overview

The F1DR8761C is compatible with Bluetooth core specification v5.3, and supports dual mode (BR/EDR+Low Energy Controllers). It is compatible with previous versions, including v2.1+EDR. For BR/EDR, it allows one active link in either slave mode or master mode. For Low Energy, it supports multiple states and allows one active link in slave mode. A BR/EDR link and an LE link can be active at the same time.

It integrates the baseband controller in a small package and supports an internal antenna, so designers can have more flexibility in product shape

F1DR8761C can be communicated by UART port.

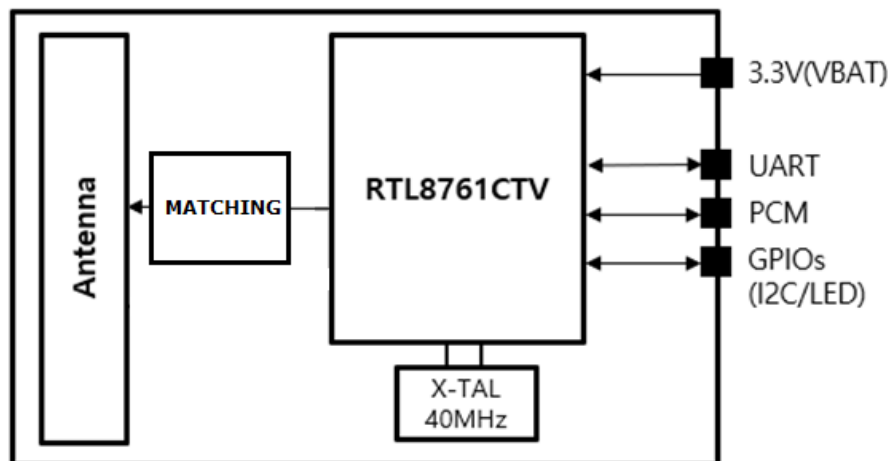


Figure1. F1DR8761C block diagram

1.2.Feature

- Bluetooth
 - Bluetooth specification Version 5.3
 - Bluetooth classic (BDR/EDR) + Low Energy (BLE)
- Integrated MCU to execute Bluetooth protocol stack
- Support LE Audio CIS/BIS Auracast
- Compatible with Bluetooth v2.1 and v3.0 systems
- TX 10dBm (typ.) maximal output power for Bluetooth classic and BLE
- Receive sensitivity: -94.5 dBm (1M BR), -94dBm (2M EDR),
-99dBm (1M BLE), -95dBm (2M BLE)
- Interface
 - PCM
 - UART
 - GPIOs
- Clock system
 - Build-in 40MHz main clock
- Supply voltage Range (2.8V ~ 3.6V)
- Operating temperature range (-20°C ~ +70°C)
- Competitive Size (11.0 mm x 16.0 mm : QFN 27Pin)

1.3.Application

- Portable devices
- IoT devices
- Audio devices (Headset, Speaker etc.)

2. Pin Definition

2.1.Pinout Diagram

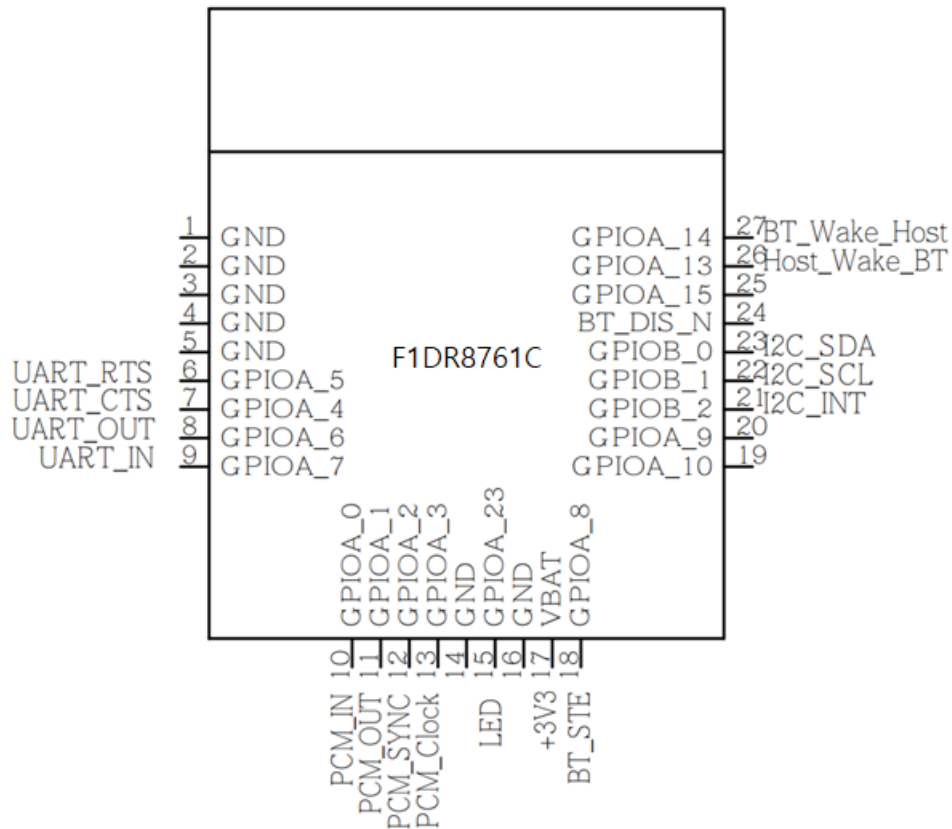


Figure2. F1DR8761C Pinout Diagram (Top View)

2.2.Device Terminal Descriptions

The symbols shown under Type indicate pin directions (I/O = bidirectional, I =input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor),

Table 1. F1DR8761C terminal descriptions

Pin	Pin Name	Pin Type	Description
1	GND	-	Ground connections
2	GND	-	Ground connections
3	GND	-	Ground connections
4	GND	-	Ground connections
5	GND	-	Ground connections
6	GPIOA_5	I/O	GPIOA_5, UART_RTS (operating votage level: 3.3V)
7	GPIOA_4	I/O	GPIOA_4, UART_CTS (operating votage level: 3.3V)
8	GPIOA_6	I/O	GPIOA_6, UART_OUT (operating votage level: 3.3V)
9	GPIOA_7	I/O	GPIOA_7, UART_IN (operating votage level: 3.3V)
10	GPIOA_0	I/O	GPIOA_0, PCM data input
11	GPIOA_1	I/O	GPIOA_1, PCM data output
12	GPIOA_2	I/O	GPIOA_2, PCM sync
13	GPIOA_3	I/O	GPIOA_3, PCM clock
14	GND	-	Ground connections
15	GPIOA_23	I/O	GPIOA_23, LED (Active Low)
16	GND	-	Ground connections
17	VBAT	I	3.3V Power Input
18	GPIOA_8	I/O	GPIOA_8, BT_STE
19	GPIOA_10	I/O	GPIOA_10, WLAN_ACT
20	GPIOA_9	I/O	GPIOA_9, BT_ACT
21	GPIOB_2	I/O	GPIOB_2, I2C_INT
22	GPIOB_1	I/O	GPIOB_1, I2C_SCL
23	GPIOB_0	I/O	GPIOB_0, I2C_SDA
24	BT_DIS_N	I	Disable Bluetooth on Negative Signals
25	GPIOA_15	I/O	GPIOA_15
26	GPIOA_13	I/O	GPIOA_13, Host_Wake_BT (Host wakeup bt signal)
27	GPIOA_14	I/O	GPIOA_14, BT_Wake_Host (BT wakeup host signal)

3. General specification

Table 2. F1DR8761C general specifications

Model Name	F1DR8761C
Product Description	BT 5.3 (Dual Mode)
Dimension	11.0 x 16.0 x 2.3 mm
BT Interface	UART / PCM
Operating temperature	-20 to + 70°C

3.1. Electrical Characteristics

3.1.1. Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Rating	Min.	Max.
Storage temperature	-40°C	+105°C
Storage Humidity	30%	60%

3.1.2. Recommended Operating Conditions

Table 4. recommended operating conditions (Ta = 20 °C)

Operating Condition	Min.	Typ.	Max	Unit
Operating temperature range	0	-	70	°C
VBAT	3.0	3.3	3.6	V
VIO	3.0	3.3	3.6	V

3.1.3. Power Consumption

Table 6. power consumption (TBD)

Operating Condition	Min.	Typ.	Max	Unit
TX, BR (DH1, PRBS9)				mA
TX, EDR (2DH1, PRBS9)				mA
TX, LE (1Mbps, PRBS9)				mA
RX, BR				mA
RX, EDR				mA
RX, LE				mA

4. Bluetooth RF Specifications

4.1. BR + EDR RF specification

4.1.1. BR + EDR Receiver

Table 11. BR + EDR receiver RF specifications(TBD)

Parameter	Condition	Min.	Typ.	Max.	Unit
Receive sensitivity with dirty transmit off	1 Mbps, GFSK BDR, 0.1% BER	-		-70	dBm
	2 Mbps, $\pi/4$ -DQPSK (2M EDR), 0.01% BER	-		-70	dBm
Maximum input level	1 Mbps, GFSK BDR	-20	-	-	dBm
	2 Mbps, $\pi/4$ -DQPSK EDR-2	-20	-	-	dBm

4.1.2. BR + EDR Transmitter

Table 12. BR + EDR transmitter RF specifications(TBD)

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency range	-	2402	-	2480	MHz
TX output power	GFSK	-	-	8	dBm
	$\pi/4$ -DQPSK (2M EDR)	-	-	7.5	dBm
Initial Carrier Frequency Tolerance	$f_0 - f_{TX}$	-25		+25	KHz
Modulation Characteristics	Δf_{1avg}	140	-	175	KHz
	Δf_{2max}	115			KHz
	$f_{1 avg} / f_{2 avg}$	80			%

4.1.3. LE Receiver

Table 11. LE receiver RF specifications(TBD)

Parameter	Condition	Min.	Typ.	Max.	Unit
Receive sensitivity: LE2 with dirty transmit off	PER $\leq$ 30.8%	-	-	-70	dBm
Maximum input level	PER $\leq$ 30.8%	-10	-	-	dBm

4.1.4. LE Transmitter

Table 12. LE transmitter RF specifications(TBD)

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency range	-	2402	-	2480	MHz
TX output power	GFSK (LE)	-	-	10	dBm
Initial Carrier Frequency Tolerance	$f_0 - f_{TX}$	-25		+25	KHz

5. Interface

5.1.UART Interface

The F1DR8761C UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115.2 Kbps.

When F1DR8761C is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

5.2.Digital Audio Interface

The F1DR8761C embeds I2S digital audio interface modules, which can be configured to connect external DSP core (or audio amplifier/audio codec). The digital audio interfaces can operate in either PCM/I2S mode or TDM mode.

5.2.1. PCM/I2S

The sampling rate is programmable for external device with I2S connection. No master clock(MCLK) can be supported for external device, and note that I2S BCLK/LRCK are jittered clock generated from XTAL source 40MHz. The EVB's I2S BCLK/LRCK clock jitter ratio measurements are as follows:

Table 13.I2S BCLK Clock Jitter Percentage

BCLK (MHz)		Clock Jitter Percentage (%)
Sampling rate 48KHz Group	1.024	1.132
	2.048	1.032
	3.072	1.772
	6.144	1.297
	12.288	1.627
Sampling rate 44.1KHz Group	2.8224	1.241
	5.6448	1.261
	11.2896	1.240

Table 14.I2S LRCK Clock Jitter Percentage

LRCK (KHz)	Clock Jitter Percentage (%)
16	0
48	0.08
96	0.179
44.1	0.107
88.2	0.114
192	0.168

- Format : I2S, Left-justified, PCM mode-A, PCM mode-B
- Configurable 16/20/24/32-bit data resolution (Audio data length)
- Configurable 16/20/24/32-bit word length (Channel length)
- Sampling rate : 192K/96K/88.2K/48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz
- Supported sampling rate up to 96KHz for programmable 4-channel TDM mode
- Supports I2S Master mode and I2S Slave mode
- Not support master clock(MCLK) output

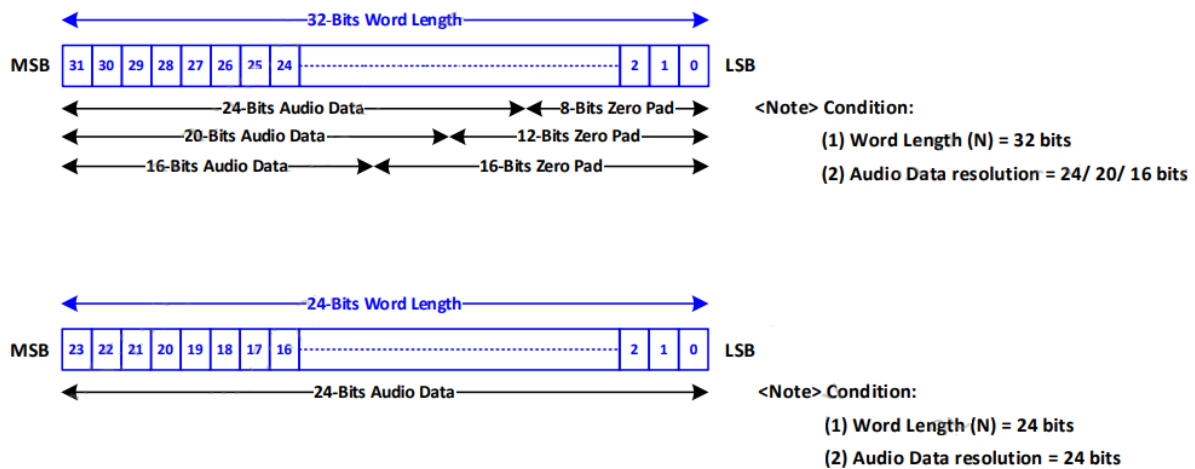


Figure4. Bit Allocations for each Channel

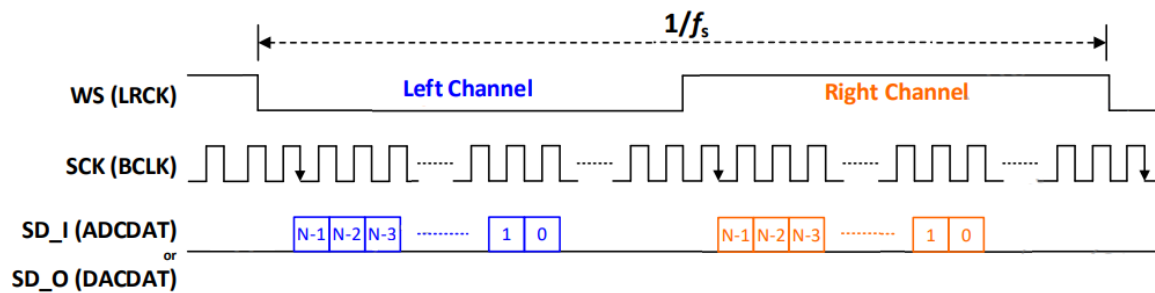


Figure5. I2S Waveform

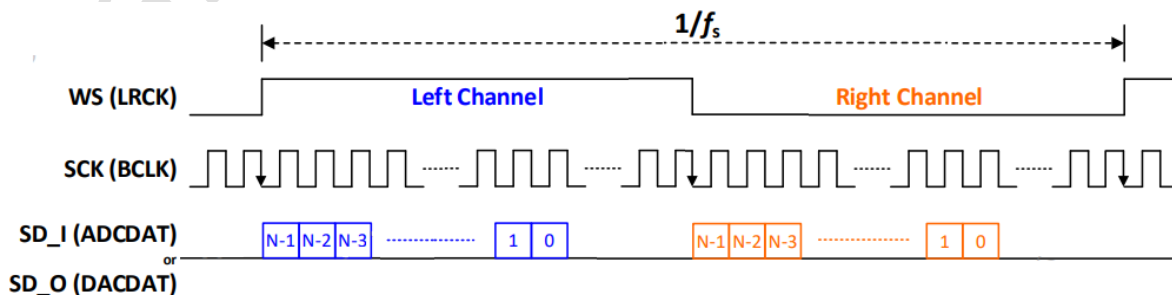


Figure6. Left-Justified Waveform

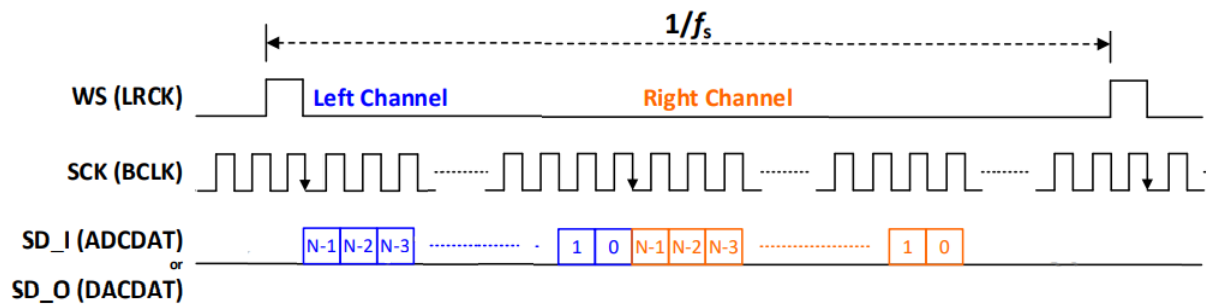


Figure7. PCM Mode-A Waveform

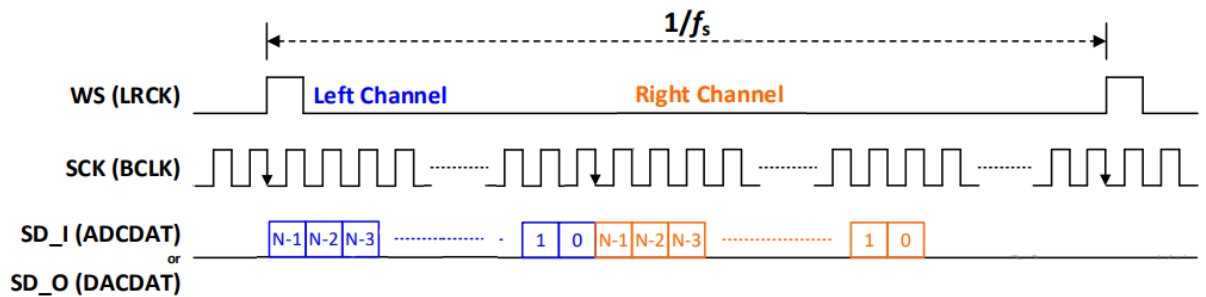


Figure8. PCM Mode-B Waveform

5.3.LED

The RTL8761C series support GPIO assignment to drive the LED for status indication.

Parameter	Min.	Typ.	Max.	Unit
Driving capacity	-	-	8	mA
GPIO V _{OH}	1.8	-	3.3	V
GPIO V _{OL}	-	0.2	-	V

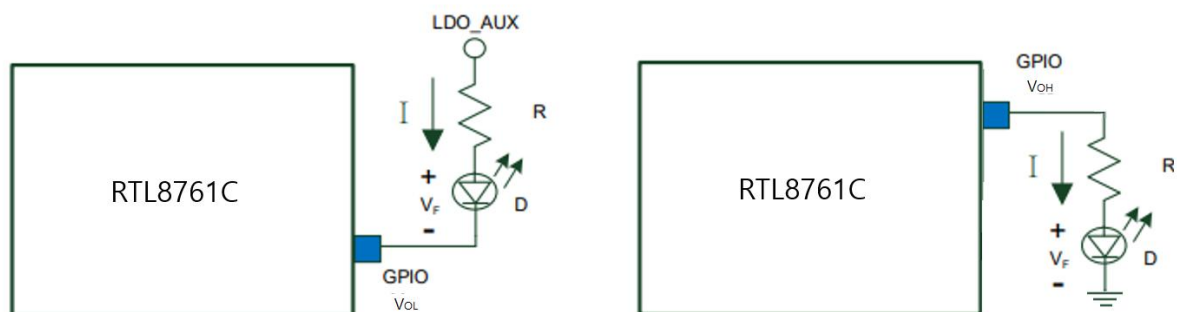


Figure5. F1DR8761C LED Sample schematic

6. Reference Schematic

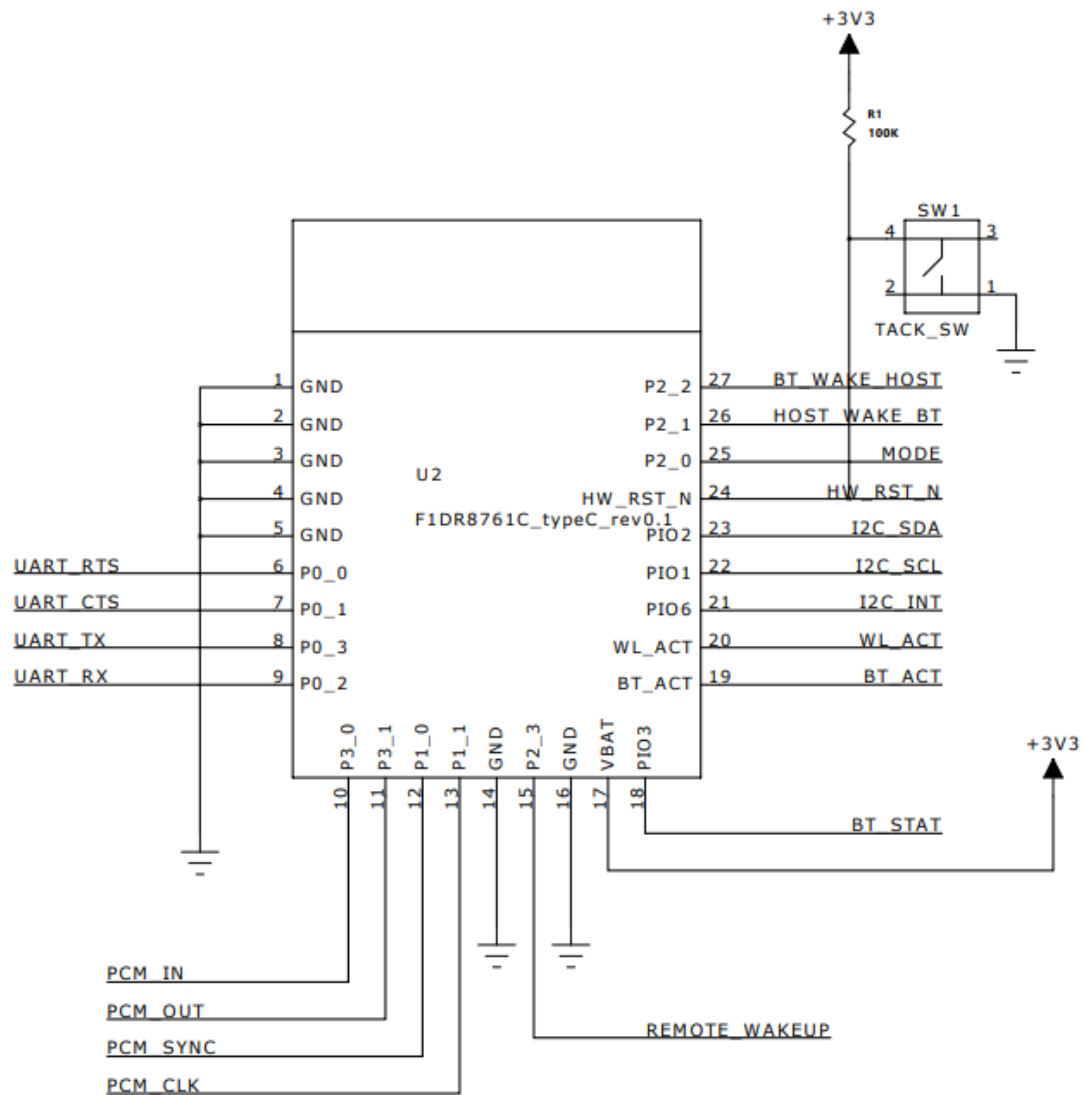


Figure6. F1DR8761C reference schematic

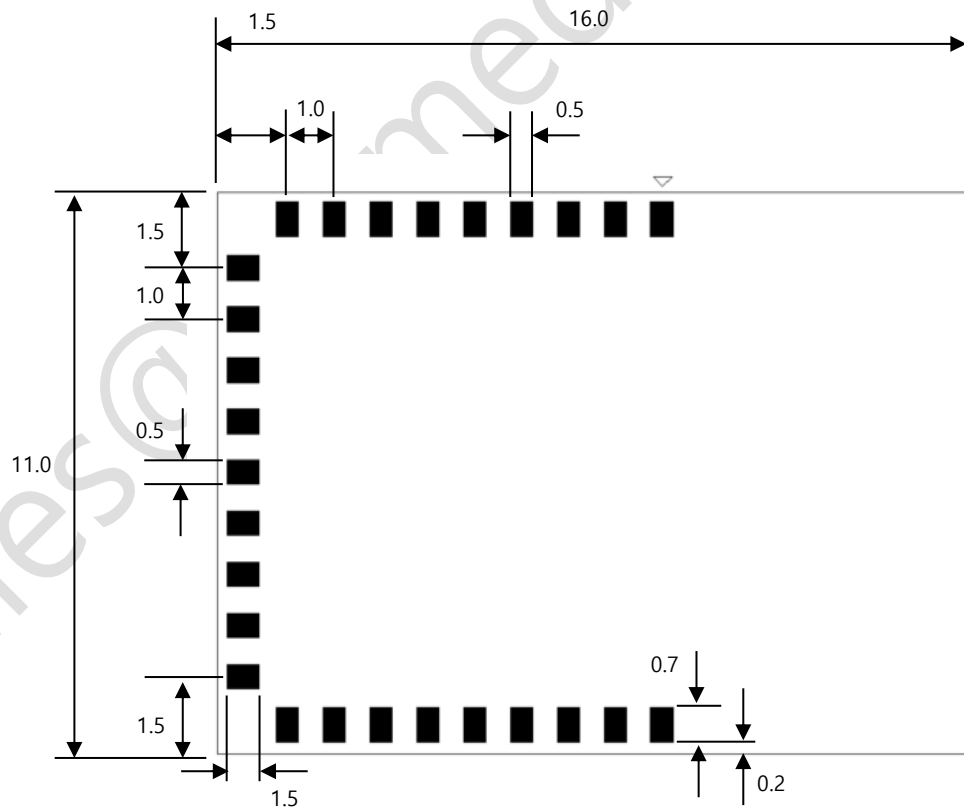
7. Dimension

7.1.Module Dimensions

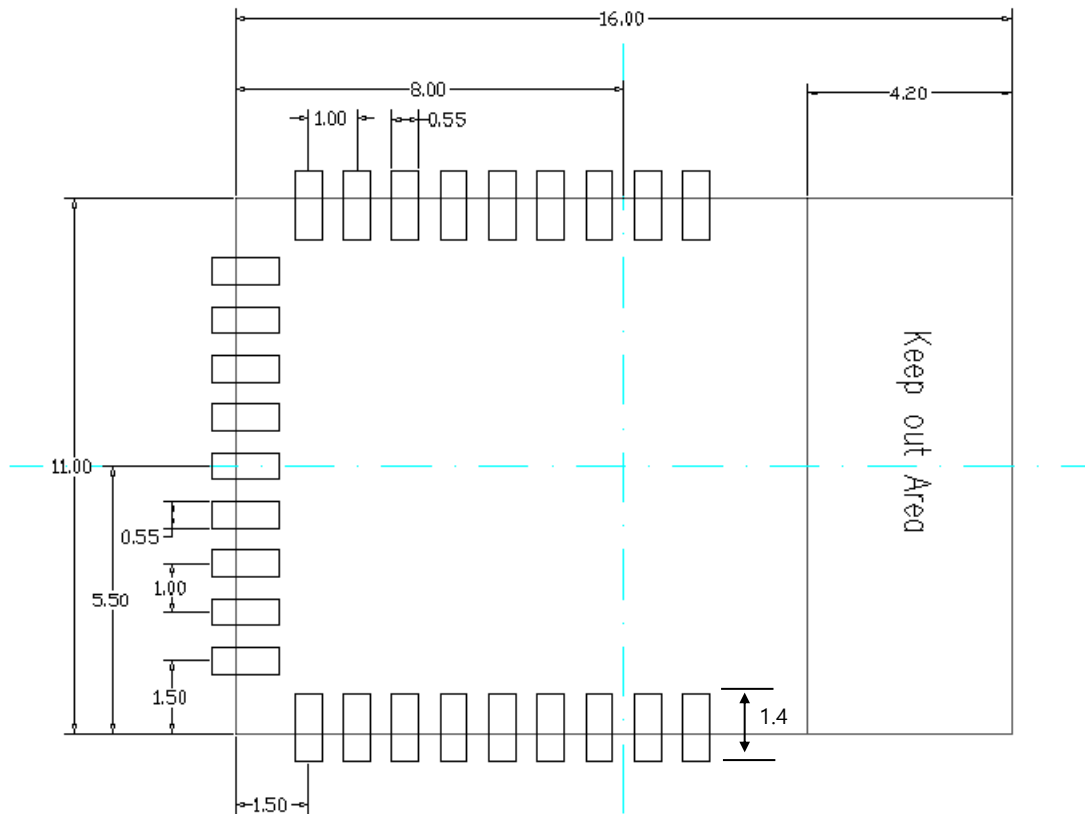


<Side View>

<Top View>

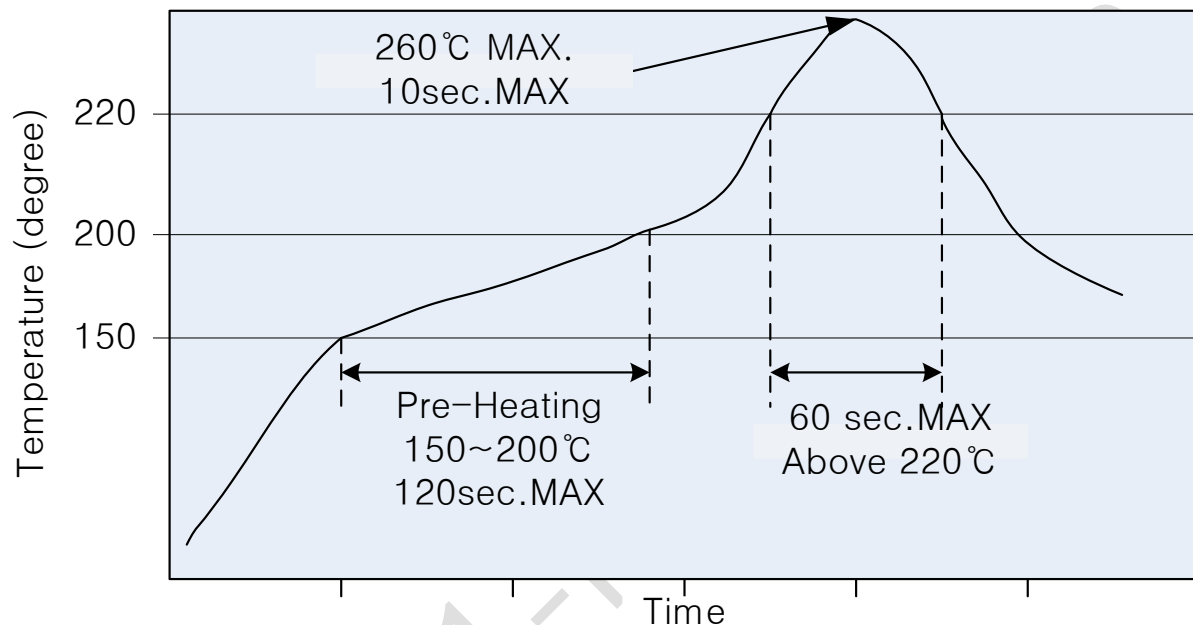


7.2.Recommended Footprint



8. Reflow Temperature Profile

Recommended solder reflow profile are shown in below and follow the lead-free profile in accordance with JEDEC Std 20C. Table lists the critical reflow temperatures. Flux residue remaining from board assembly can contribute to electrochemical migration (ECM) over time. This depends on a number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins. Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.



Process Step	Lead-Free Solder
Pre-Heat	150~200°C
Pre-Heat Time	MAX 120 sec.
Time above liquidus	Above +220°C. MAX 60 sec
Peak temperature	MAX +260°C
Time within 5°C of peak temperature	MAX 10 sec

9. Module Placement Rule

On the main PCB, the areas under the antenna should not contain any top, inner layer, or bottom copper as shown in Figure. In all cases, the performance of the antenna can vary depending on GND.

