

WA20-6829B

USER MANUAL

Confidential

Table of Contents

1. Overview	4
1.1. WA20-6829B EVM and Controller Features	5
2. Installation	6
2.1. EVM Installation.....	6
2.2. Using the EVM Software	7
2.2.1. Installed Program file list.....	7
2.2.2. The GUI guideline for the EVM.....	7
2.3. Configuration of GUI (Control program)	8
2.3.1. Main window.....	8
2.3.2. Input menu part	11
2.3.3 Volume	13
2.3.4 DRC	15
2.3.5 Filter design	17
2.3.6 Filter design (APEQ)	18
2.3.7 ReBass.....	19
2.3.8 Filter design sequence.....	19
3. Initialize sequence.....	20
3.1 Recommended software control	20
3.2 Initialize: typical example	21
4. Description DRC & Prescaler	27
4.1. DRC.....	27
4.1.1. Definition.....	27
4.1.2. Threshold	27
4.1.3. Attack & Release Time	27
4.1.4. Gain curve	28
4.1.5. 1Band DRC structure	28
4.1.6. Two Band DRC structure.....	29
4.1.7. Three Band DRC structure	30
4.1.8. QMF(Quadrature Mirror Filter).....	30
4.1.9. DRC Setting sequence	31
4.1.10. Designed QMF Graph.....	32
4.1.11 Setting sequence	33
4.2 Pre-scaler	36
4.2.1 Definition.....	36
5. ReBASS	37
5.1 ReBASS Control.....	37
5.2 ReBASS Structure	37
5.3 ReBASS Setting	38
6. Hardware.....	41
6.1. Recommended circuit.....	41

6.2. Power sequence	42
6.3. Output power for PVDD	43
6.4. Output Filter-design	44
7. Trouble shooting guide	45
7.1. Check Flow	45
7.2. Checking circuit for sound quality	46
7.3. Checking power circuit	47
7.4. Checking output	47
7.5. Checking Software (Control Program)	47
7.6. Checking input	48

Confidential

1. Overview

The WA20-6829B EVM evaluation module includes necessary information to run WA20-6829B audio amplifier. The two bridge-tied load (BTL) configurations are employed in the EVEM board, and the design of WA20-6829BEVM can be used as a reference for LCD TVs, Mini audio components, and other audio solutions.

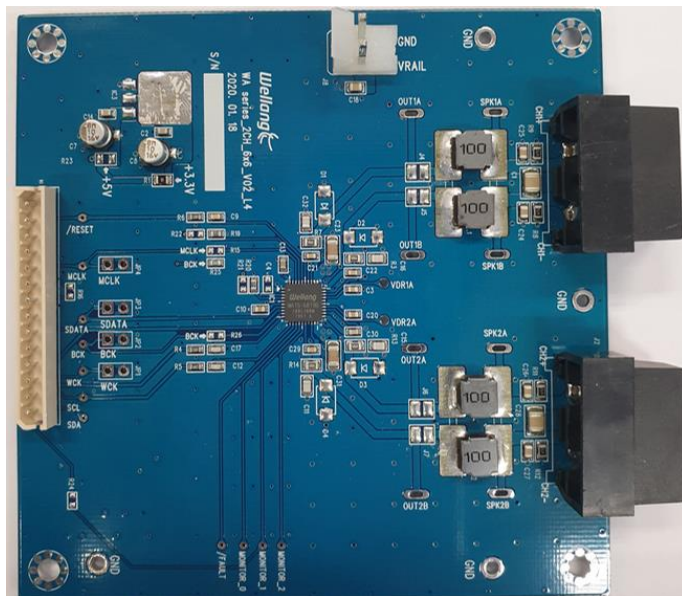


Figure 1. WA20-6829B EVM Printed-Circuit Board

The evaluation system with the controller board implements a 2-channel digital audio amplifier system. The controller board has functions like USB interface, digital audio input (SPDIF), ADC for analog input, mute control, and voltage regulation.

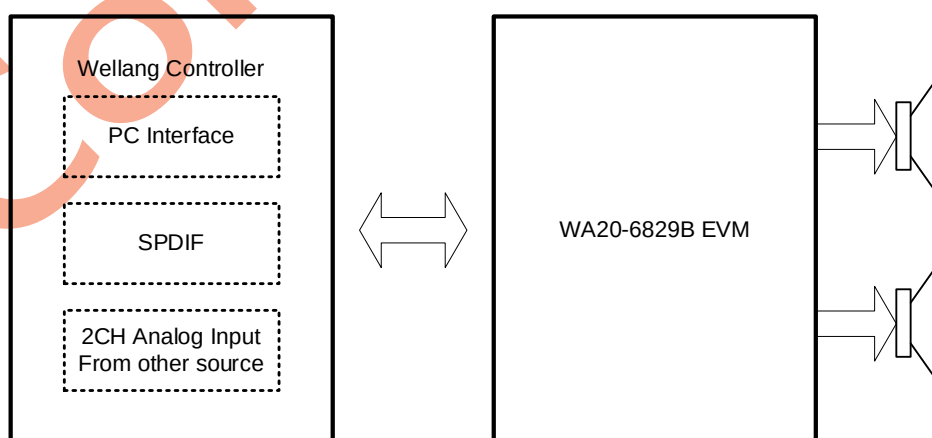


Figure 2. Complete System and EVM Signal Path Overview

1.1. WA20-6829B EVM and Controller Features

- 2 CH Stereo Config
- SDATA Generator (I²S Output)
- USB Interface
- I²S Input (Coaxial Input)
- Analog input (ADC AK5386)
- 4Layer PCB
 - Controller : size(65mm x 95mm), 1.6T
 - WA20-6829B EVM : size(95mm x 95mm), 1.6T

Confidential

2. Installation

This section explains how to install the hardware and the software.

2.1. EVM Installation

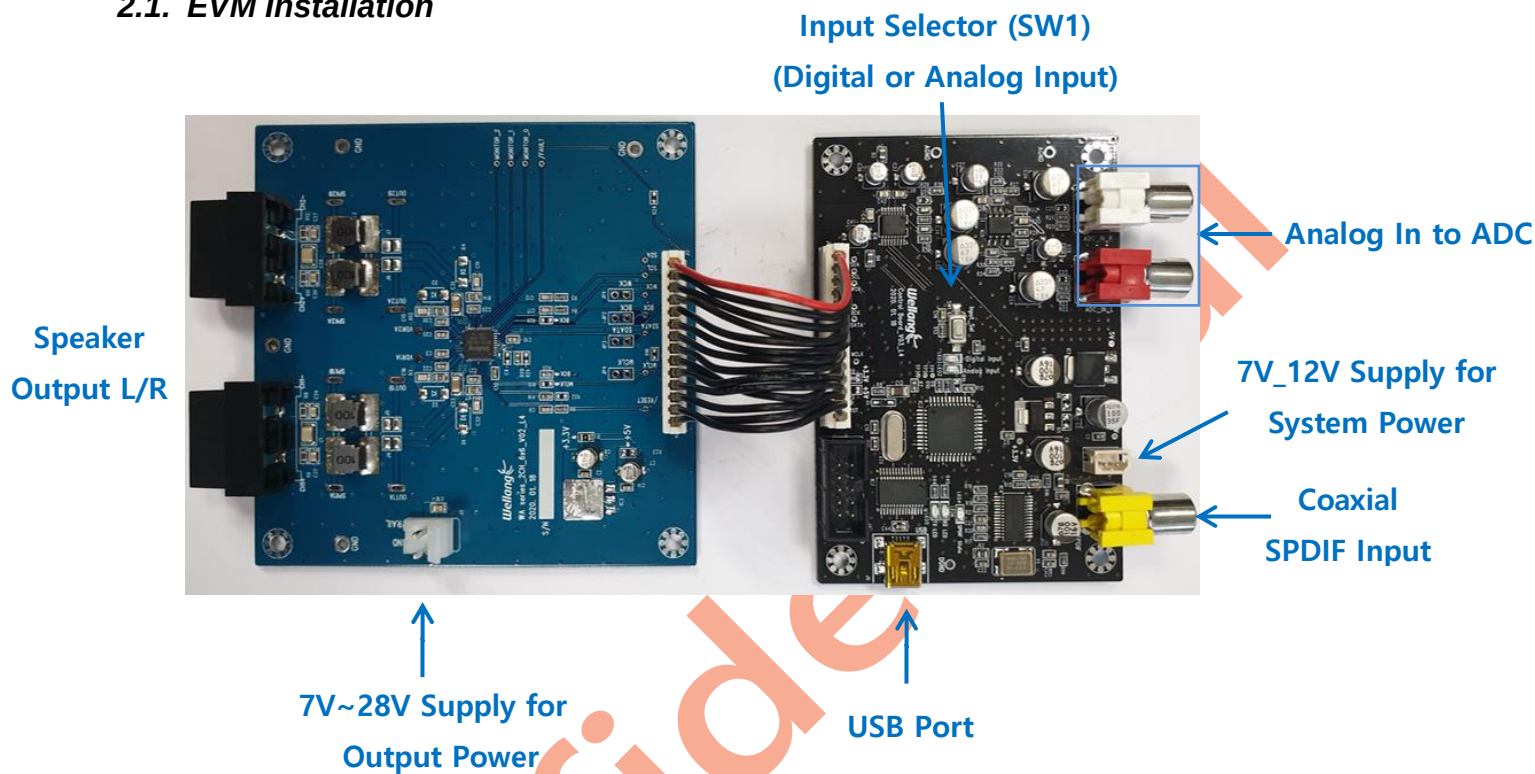


Figure 3. WA20-6829B Connection

- Initial setting for EVM B/D
 - ① Connect a power source (7V~12V, 1A) to the controller board.
 - ② Connect another power source (7V ~ 28V) to VRAIL(PVDD).

Note: The power source for WA20-6829B should be able to supply more than 4A current for maximum power output and stable operation.
 - ③ Connect a 6~8Ω speaker or a dummy load for L-CH
 - ④ Connect a 6~8Ω speaker or a dummy load for R-CH
 - ⑤ Connect the PC and the Control Board of the WA20-6829BEVB KIT using a USB cable.
 - ⑥ Run the control software on the PC (WA20-6829B CP).
 - ⑦ Press the Input selector (SW1) of the Control Board to select the input

2.2. Using the EVM Software

The key features of WA20-6829B are Parametric EQ(PEQ), Advanced parametric EQ(APEQ), Dynamic range compression (DRC), volume control, mixer, etc. The control program (CP) with GUI running on the PC can control all functions of WA20-6829B via I²C. The CP runs.

To install the CP, run WA20-6829B_setup.exe on the USB or CD provided.

2.2.1. Installed Program file list

If the CP is installed properly, you can find the following files in the installed directory (e.g. C:\Program Files\Wellang\WA20-6829B).

File List: 6 files

Default.cfg	- Initializing settings for 2 channels
Default #2.cfg	- Another amp(#2) initializing settings for 2 channels
PowerMeterGain.cfg	- Gain coefficient for power meter
WA20-6829B-A.exe	- Execution file
SOUNDOFF.cfg	- Settings for sound off sequence
SOUNDON.cfg	- Settings for sound on sequence

The CP can run predefined commands using script
CFG files can be edited using text editors like notepad.

2.2.2. The GUI guideline for the EVM

- ① Connect a power supply to the EVM board as well as the controller board.
- ② Connect audio input to the audio input of the EVM board.
- ③ Connect speakers to the output of the EVM board.
- ④ Connect a USB cable between the PC and the controller board.
- ⑤ Turn on the power supply.
- ⑥ Check the COM port of the PC and set the proper number of the serial port in the CP.
- ⑦ Read the 0x00 register value. If 0x00 value is read, the connection is correctly

2.3. Configuration of GUI (Control program)

2.3.1. Main window

If you run WA20-6829B.exe, you will see the Figure 4.

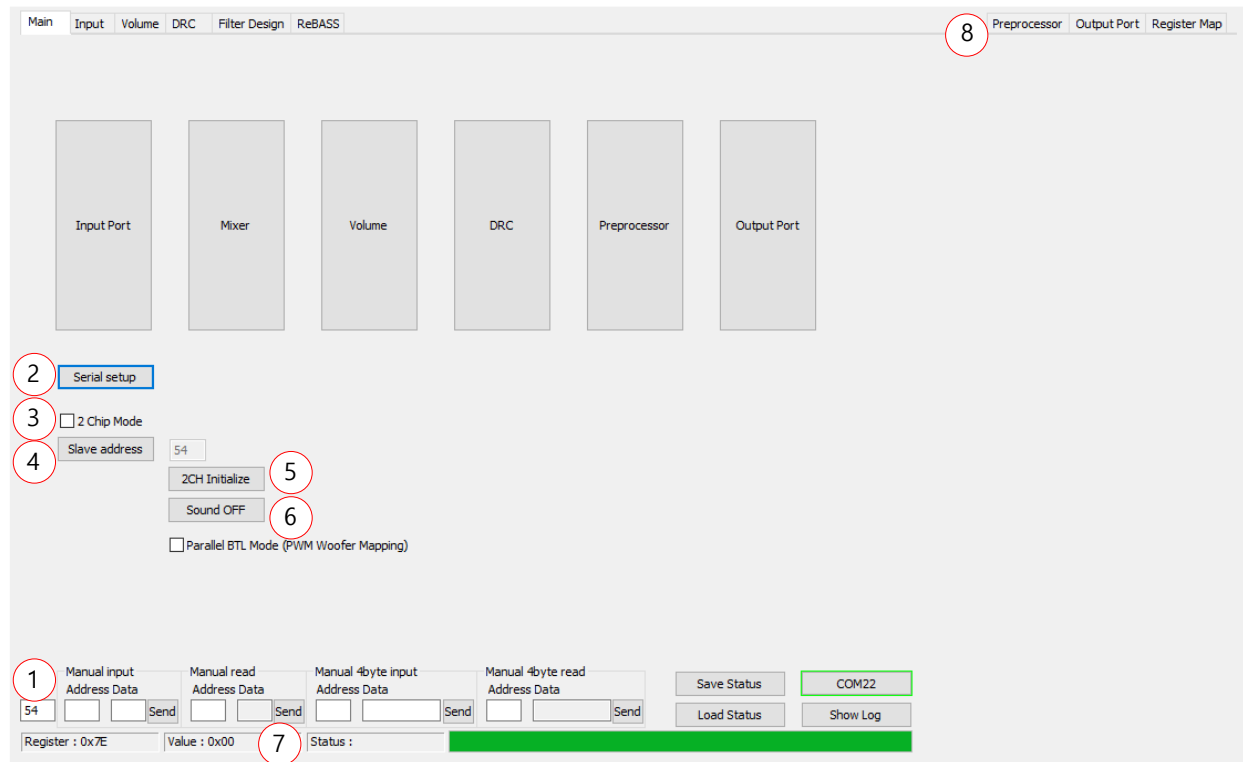


Figure 4. WA20-6829B Control program (CP) main window

① Manual input

Figure 5 shows the manual command section. The following explains how to use each manual command input.

- ① Input register address and data in each blank, and click 'Send' button.
- ② If the data size is 1 byte, use 'Manual Input'.
- ③ If the data size is 4 byte like the coefficients of the Biquad filters, use 'Manual 4byte Input'. Please note that the whole set of 5 coefficients for each Biquad filter should be written to apply the coefficients. Writing only one out of five coefficients does not update the register in the 4 byte writing.
- ④ For convenience, using a scrip file is recommended for setting 4 byte data.
- ⑤ Save Status : saves the status of currently applied CP register values.
- ⑥ Load Status : restore already saved register values of CP

Manual input		Manual read		Manual 4byte input		Manual 4byte read			
Address	Data	Address	Data	Address	Data	Address	Data	Save Status	Disconnected
54								Load Status	Show Log
Register : 0x68		Value : 0x00		Status :					

Figure 5. Manual input & read section

② Serial setup

Click 'Serial Setup' button can set parameters for serial communication as shown in Figure 6. After completing Port Setup, press the OK button to change the portion marked Disconnected to the Port you set.

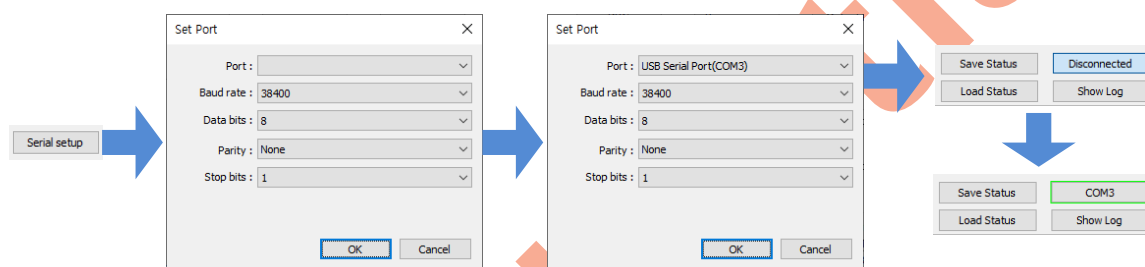


Figure 6. Serial setup

③ 2Chip Mode

If two amplifier chips are to be used, '2CHIP MODE' should be checked as shown in the following figure. For this mode, the system hardware configuration should be properly made; the AD pin of one chip is low (slave address 0x54), and the AD pin of other chip is high (slave address 0x56).

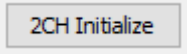


④ Slave address

The default slave address of I²C for WA20-6829B when the AD pin is GND is 0x54. However, if the AD pins is high, the slave address becomes 0x56.

⑤ File download for Initializing

'2CH Initialize' button can download the scrip file, default.cfg, from the installed directory (e.g. C:\Program Files\Wellang\WA20-6829B).

A rectangular button with a light gray background and a thin border, containing the text "2CH Initialize" in a dark gray font.

⑥ Sound On / Off

If you click 'Sound On/Off' button, SoundON.cfg or SoundOFF.cfg script file is downloaded from the installed directory.



⑦ Bottom value of main menu

It shows the data and the register value currently transmitted and activated in WA20-6829B

Register : 0x68	Value : 0x00	Status :
-----------------	--------------	----------

⑧ Preprocessor, Output Port, Register Map

The functions of the Preprocessor, Output Port, and Register Map Tab are used when debugging.

2.3.2. Input menu part

If you click 'Input' tab in the main window of the CP, the following input window appears as shown in Figure 7. The default values are shown as well.

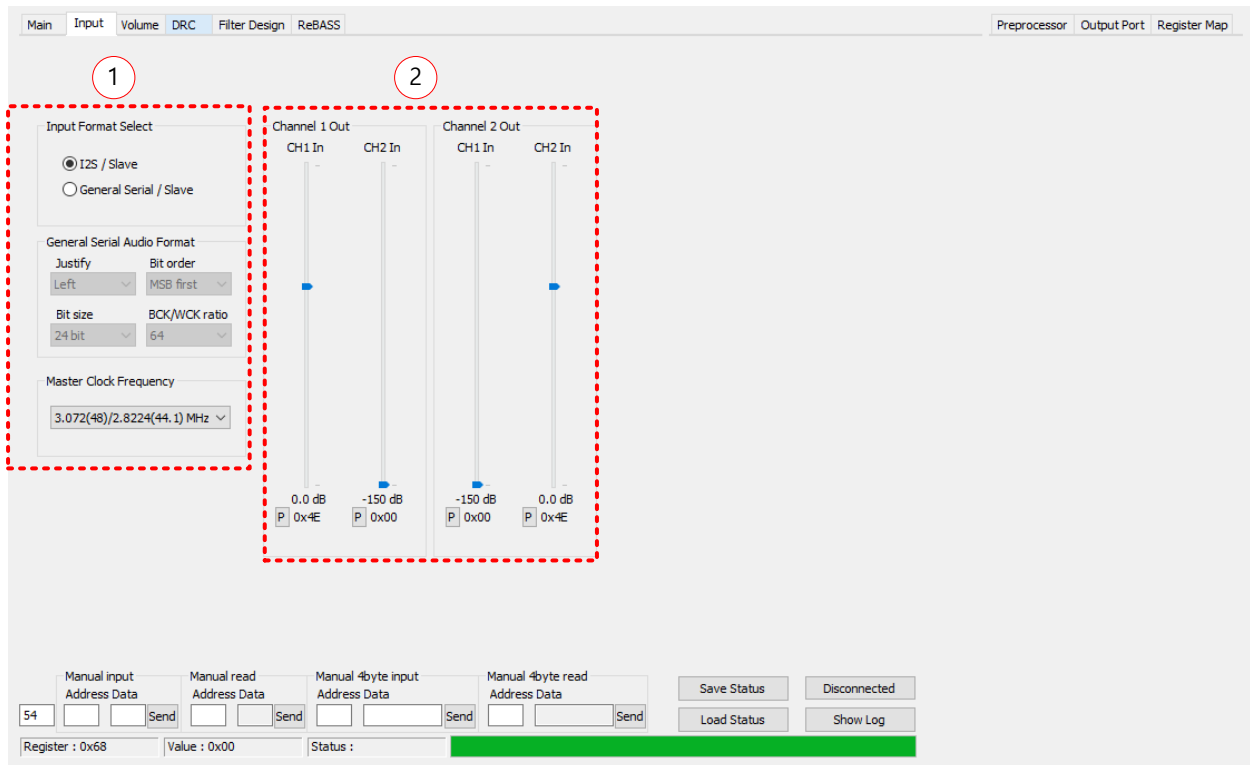


Figure 7. Input port setting

① Input format selecting

Section name	EVM default	Register
Audio input format & Mode	I2S slave mode	0x00
General Serial audio format		0x00
Input sampling frequency	48kHz, manual select mode	0x00
Master Clock Frequency	3.072MHz / 2.8224MHz	0x00

② Mixer

Mixer has four gain values (M00~M11) [Figure 7-②], and its value can be changed while composing a matrix output of both channels. Please refer to Appendix A in the datasheet of WA20-6829B to set the gain value.

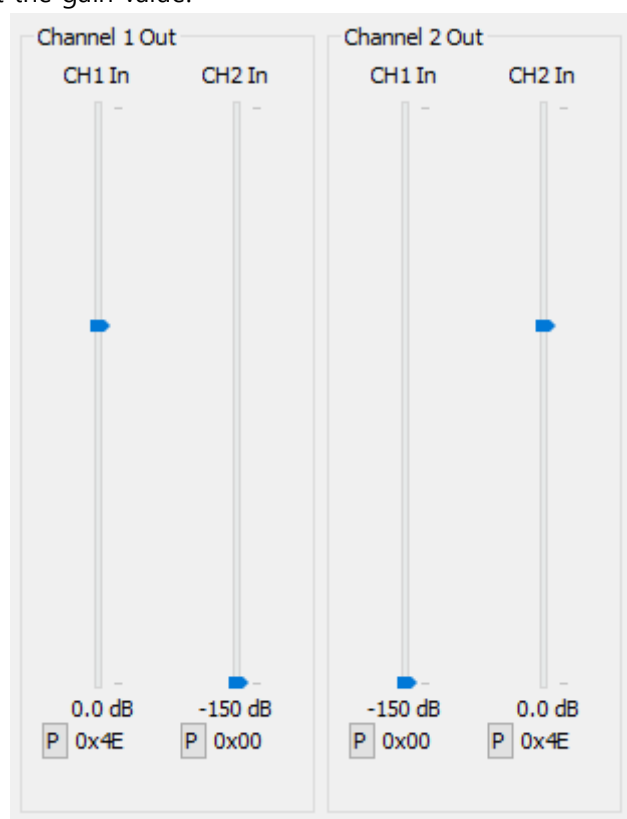


Figure 8. [2X2] Mixer setting

$$\begin{bmatrix} CH1\ Out \\ CH2\ Out \end{bmatrix} = \begin{bmatrix} M00 & M01 \\ M10 & M11 \end{bmatrix} \cdot \begin{bmatrix} CH1\ In \\ CH2\ In \end{bmatrix}$$

$$[\text{Output Channels}] = [\text{Mixer Matrix}] \times [\text{Input Channels}]$$

Section name	EVM default	Register
Gain control (M00)	0dB (positive)	0x03
Gain control (M01)	-infinity	0x04
Gain control (M10)	-infinity	0x05
Gain control (M11)	0dB (positive)	0x06

Table 1. Mixer matrix

2.3.3 Volume

Figure 9 shows the display when 'Volume' tab is clicked in the main window.

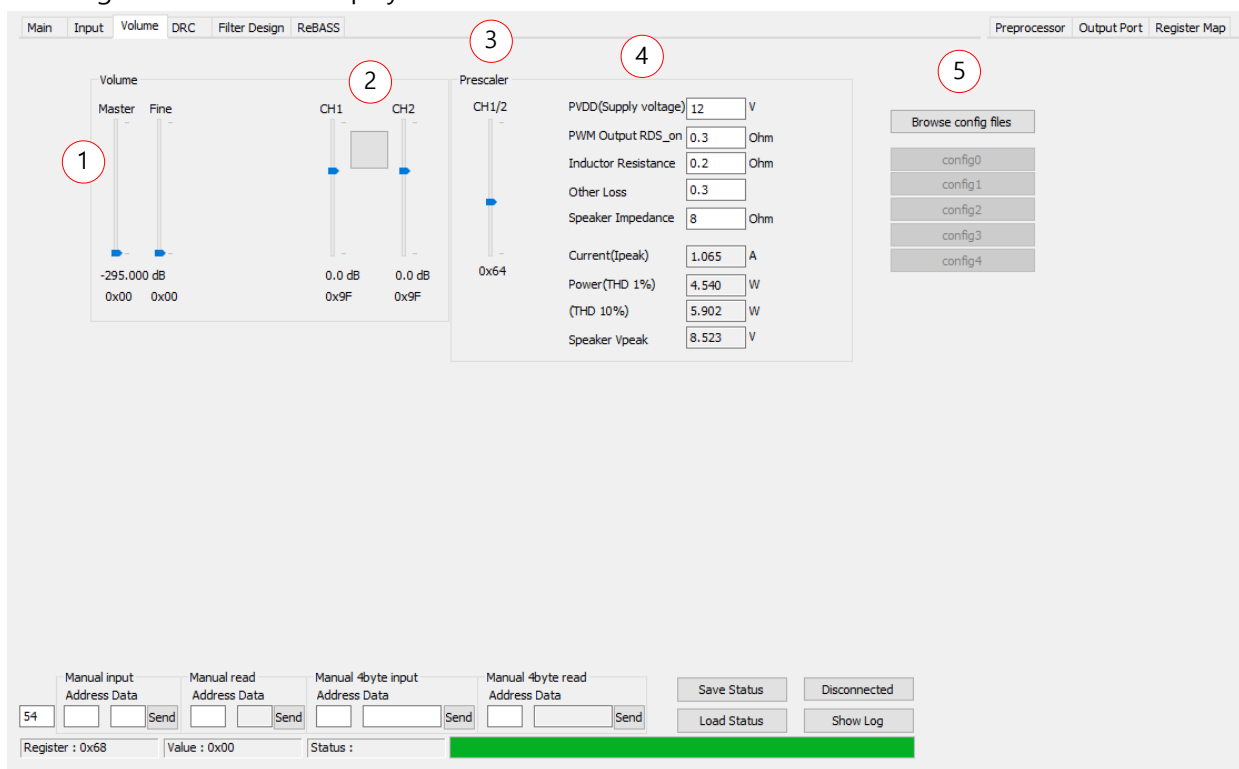


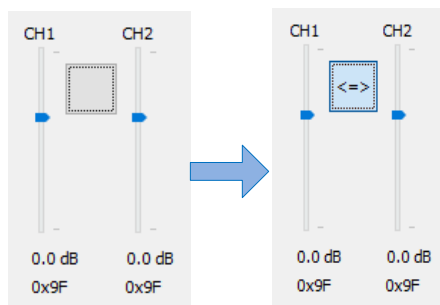
Figure 9. Volume

① Master Volume

WA20-6829B has a master volume range of -125.5dB ~ 0dB. The master volume controls CH1 and CH2 at the same time, and the channel volume controls each channel separately.

② Chanel Volume

WA20-6829B has a channel volume range of -295dB ~ 48dB. CH1 and CH2 can be controlled separately, and if both channels are to be controlled at the same time, check the blue square as shown in the following figure



③ **Prescale Value**

Prescaler limits the maximum width of PWM pulse according to the preset level. Adjusting the Prescaler value can effect as changing PVDD voltage to manipulate maximum power output under the fixed PVDD supply. Therefore, the Prescaler value is useful when variant models of different maximum power outputs are developed with the same design platform.

④ **Power simulation**

If information such as PVDD and speaker impedance is input, the output power at THD 1% or 10% is simulated and displayed.

⑤ **Browse config file**

'Browse config files' button is a function to download predefined script files selectively. When there are several script files that are made by users, Click the 'Browse Settings File' button and select the folder containing the script file to be applied, and the files in the folder will be downloaded to the amplifier.

Confidential

2.3.4 DRC

Figure 10 shows the display when 'DRC' tab is clicked in the main window.

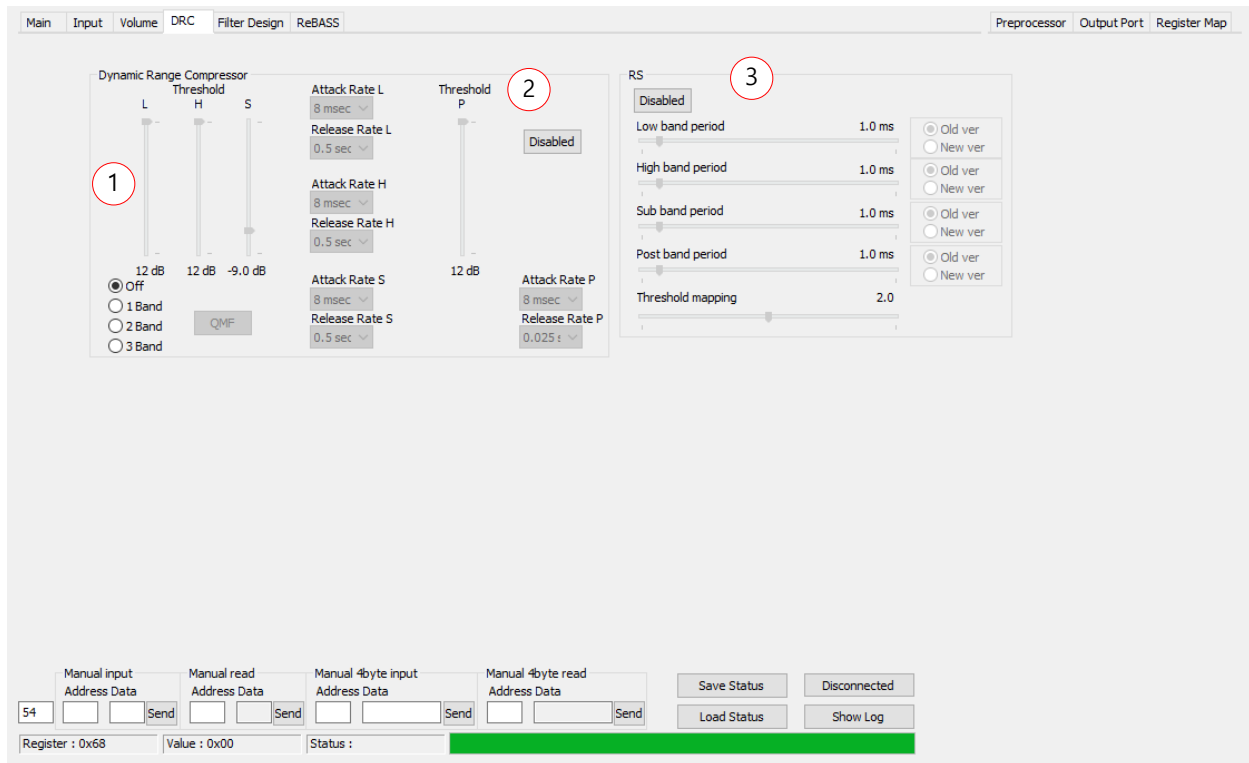


Figure 10. DRC

① DRC(Dynamic Range Compression)

DRC is a function that prevents clipping output. It also protect speakers from damage caused by an over powered signal. Figure 10-① is a section for DRC parameters. Please refer to WA20-6829B datasheet.

- ① Threshold : signal level to be limited
- ② Attack rate : decay time to Threshold level
- ③ Release rate : restoration time to unaffected input level

To minimize audible artifact, fast attack time and slow release time are recommended.

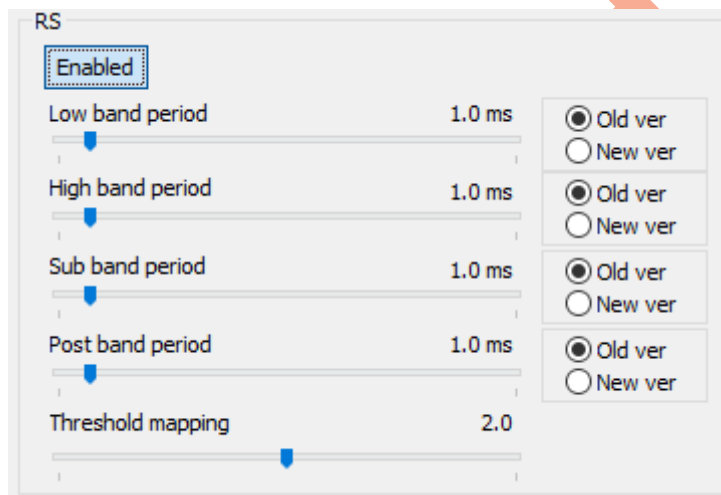
② Post DRC

Post DRC is a one band DRC that adjust overall gain after multi-band DRC (2-band or 3-band).

③ RS DRC (Reinforced Sound DRC)

RS DRC is a function that operates to reinforce the sound. RS DRC controls its gain based on RMS (Root-Mean Square) level detection.

- ① Disabled / Enabled : Clicking this button the RS DRC Enable or Disable
 - If you enable RS DRC mode, the attack parameters of Old DRC are unavailable.
- ② Low band / High band / Sub band / Post period : Attack time control for 3 band DRC & Post DRC (Range : 0.1ms~82.9ms)
- ③ Old ver / New ver : You can choose between old version & new version(RS DRC).
 - It is used to check the difference between the old version and the new version(RS DRC).
- ④ Threshold Mapping : The Threshold Mapping is to adjust the RS DRC gain.



2.3.5 Filter design

Clicking 'Filter Design' tab in the main window shows the filter design tool as shown in Figure 11.

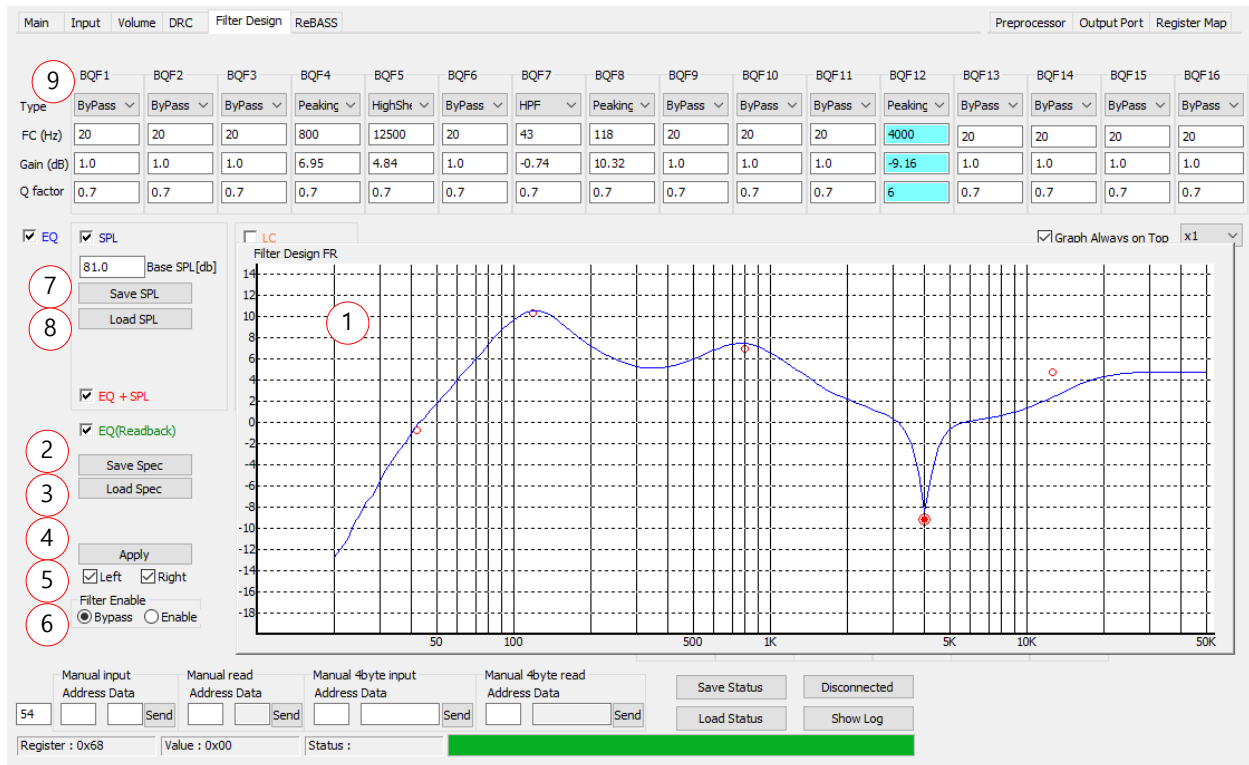


Figure 11. Filter Design window

- ① Graph window according to PEQ Setting (Filter type, Fc[Hz], Gain[dB], Q factor)
- ② Save Spec File : save current setting values of BQ1 ~ BQ16 to a file [Filter type, Fc, Gain, Q factor]
- ③ Load Spec File : restore already saved setting files of BQ1 ~ BQ16 [Filter type, Fc, Gain, Q factor]
- ④ Apply : apply the current setting values to the amplifier chip
- ⑤ Selective write to L/R channel
- ⑥ Enable or Disable all BQ filters
- ⑦ Save SPL : The value of the current graph window is saved as SPL (Sound Pressure Level) Data.
- ⑧ Load SPL : The SPL (Sound Pressure Level) data of the speaker is loaded and displayed in the graph window.

2.3.6 Filter design (APEQ)

If you move the graph window by pressing the left button of the mouse, you can see the low pass filter design and APEQ setting below as shown in Figure 12.

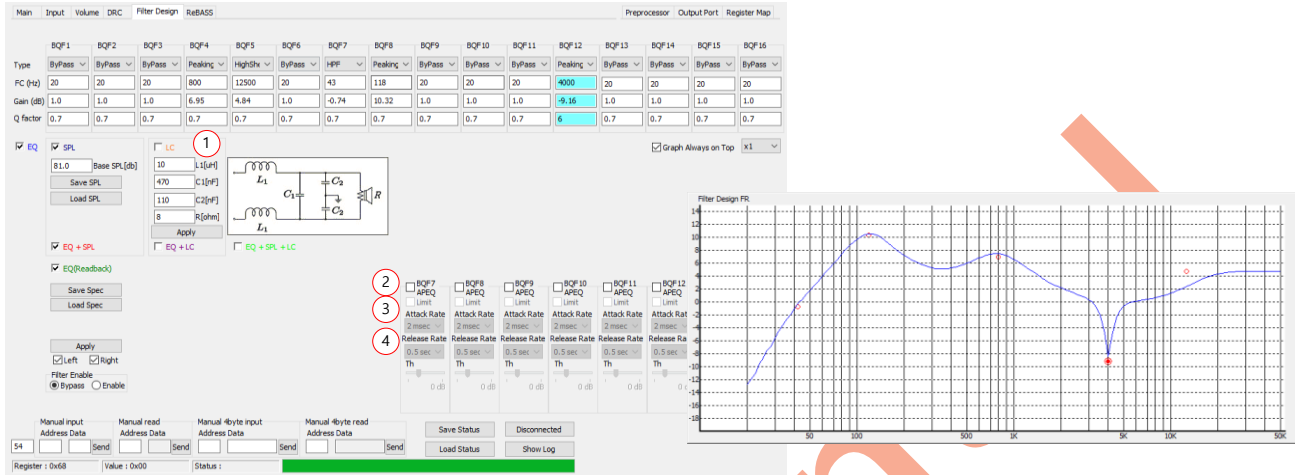
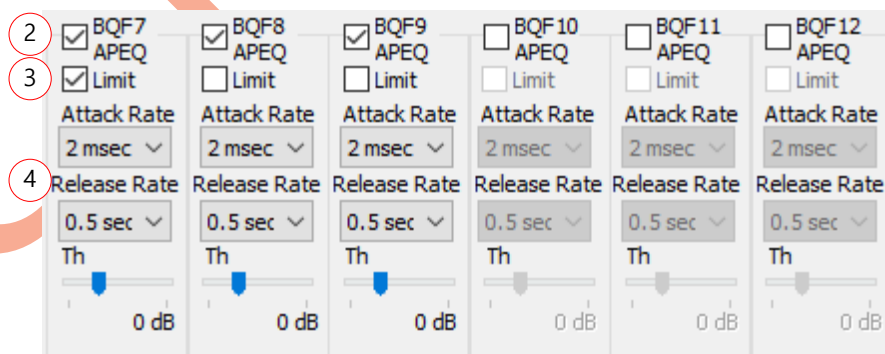


Figure 12. Filter Design window

- ① Activate low pass filter design window
- ② APEQ check box : enable APEQ function
- ③ Limit : when the signal exceeds Threshold, APEQ limit the output level
- ④ Advanced PEQ Control
 - Attack rate : response time to reduce the signal gain to Threshold level
 - Release rate : response time to return the signal gain to normal level

Generally, fast attack rate and slow release rate are recommended

 - Threshold : when the signal exceeds Threshold, APEQ reduces gain to this level



2.3.7 ReBass

Clicking 'ReBass' tab in the main window shows the filter design tool as shown in Figure 13.

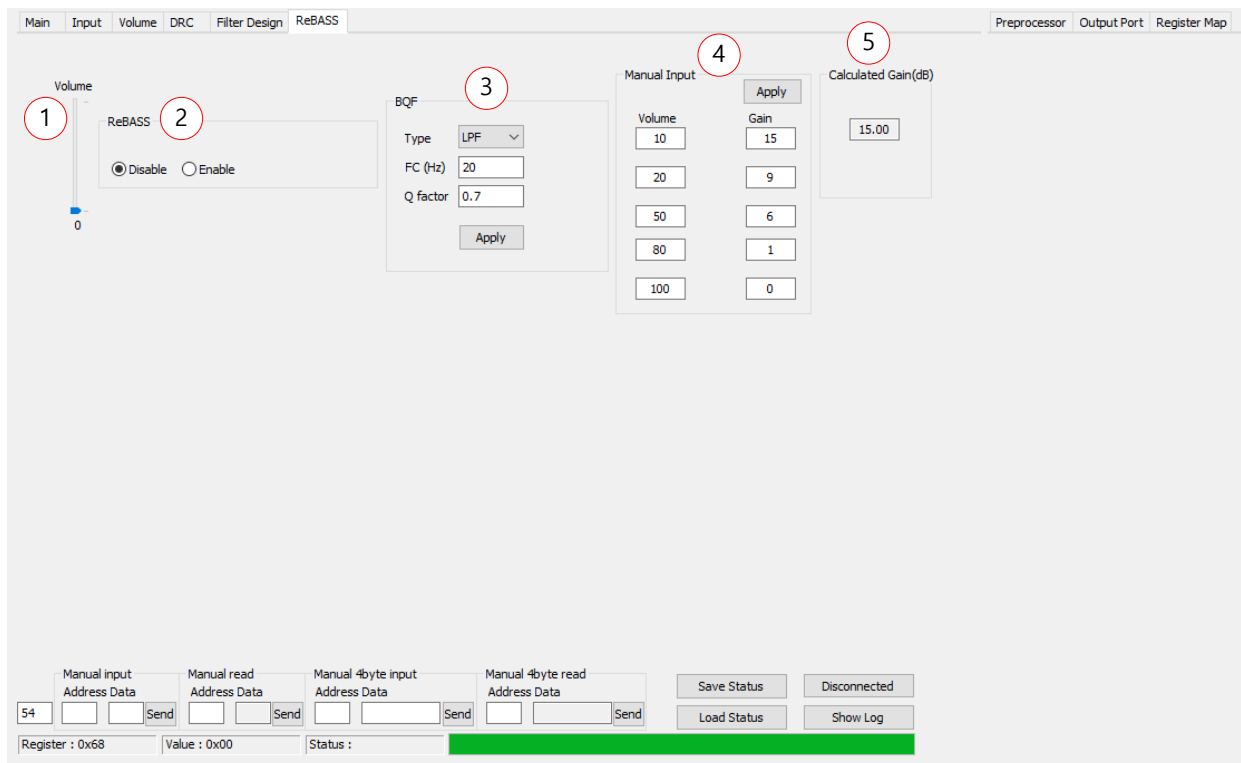


Figure 13. ReBass Design window

- ① WA20-6829B has a TV Set volume range of 0 ~ 100.
- ② Enable or Disable ReBASS check box
- ③ BQ Filter Setting (Filter type, Fc[Hz], Q factor)
- ④ After setting the desired TV volume and gain value, press the Apply button to apply it.
- ⑤ Calculated Gain(dB) : When adjusting the TV volume, the calculated gain value is displayed.

2.3.8 Filter design sequence

Following procedure illustrates how to use Filter Design.

- A. Click 'Filter Design' tab and 'Filter Design' window appears
- B. Select 'Filter type' and set Q-factor, Gain and center frequency
- C. Likewise, set all PEQs(BQ1-16) parameters, and check 'Write to' for target channels
- D. Click 'Apply' button to apply the setting values to WA20-6829B
- E. Above procedure download the register values for the target filter design and GUI displays the target frequency response

3. Initialize sequence

3.1 Recommended software control

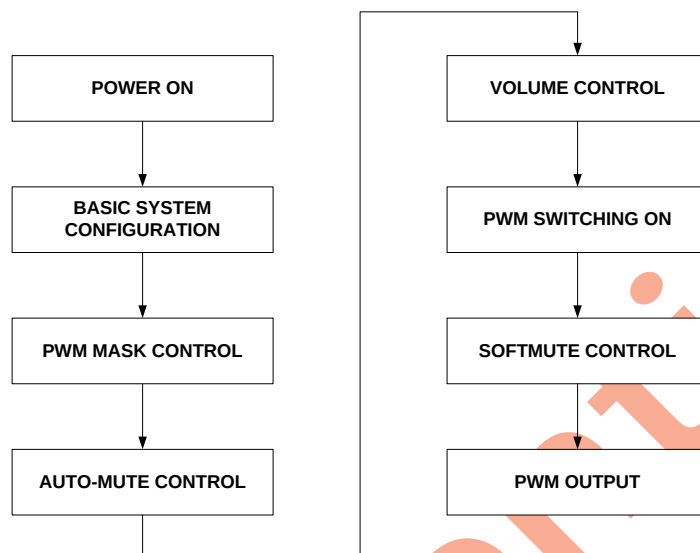
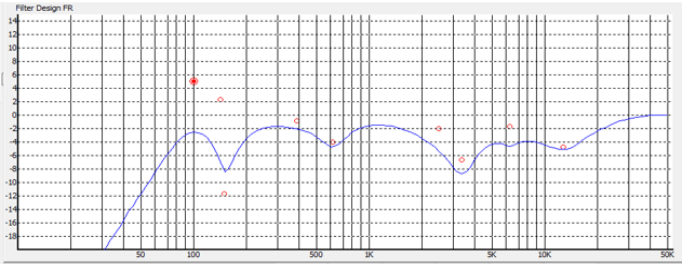


Figure 14. Initialization control flow

3.2 Initialize: typical example

No	Register	Setting Value	Description
1	0x0B	0x01	Soft Reset control
2	0x02	0x00	48k sample rate : 0x00(default), 96k sample rate: 0x01
3	0x33	0x03	Soft Mute On Control
4	0x7E	0x03	Set 4-byte I2C Mode (Enable coefficient write for ch1/ch2)
5	0x32	0x0C7BF3C4	DRC QMF_BQ1
	0x33	0x0C7BF3C4	
	0x34	0x20000000	
	0x35	0x10608188	
	0x36	0x20000000	DRC QMF_BQ2
	0x37	0x0903947F	
	0x38	0x0A03947F	
	0x39	0x0903947F	
	0x3A	0x116E42A2	DRC QMF_BQ3
	0x3B	0x10E0A1E8	
	0x3C	0x107040C4	
	0x3D	0x10F040C4	
	0x3E	0x20000000	DRC QMF_BQ4
	0x3F	0x10608188	
	0x40	0x20000000	
	0x41	0x106F49CB	
	0x42	0x11EF49CB	DRC QMF_BQ5
	0x43	0x106F49CB	
	0x44	0x116E42A2	
	0x45	0x10E0A1E8	
	0x46	0x092010AB	DRC QMF_BQ6
	0x47	0x092010AB	
	0x48	0x20000000	
	0x49	0x107D7FBD	
	0x4A	0x20000000	DRC QMF_BQ7
	0x4B	0x11000000	
	0x4C	0x20000000	
	0x4D	0x20000000	
	0x4E	0x20000000	DRC QMF_BQ8
	0x4F	0x20000000	
6	0x7E	0x00	Set 1-byte I2C Mode (Disable coefficient write for ch1/ch2)
7	0x33	0x00	Soft Mute Off Control

8	0x20	0xA8	low band DRC threshold = 0dB
9	0x21	0x10	low band DRC attack time = 4ms / release time = 1sec
10	0x22	0xA8	high band DRC threshold = 0dB
11	0x23	0x10	high band DRC attack time = 4ms / release time = 1sec
12	0x26	0x9E	Post DRC threshold = 1dB
13	0x27	0x10	Post DRC attack time = 4ms / release time = 1sec
14	0x2A	0xA8	sub band DRC threshold = 0dB
15	0x2B	0x11	sub band DRC attack time = 8ms / release time = 1sec
16	0x29	0x11	2Band DRC mode enable
17	0x2C	0x01	Sub band mode enable
18	0x17	0xBD	channel 1 vol 15dB
19	0x18	0xBD	channel 2 vol 15dB
20	0x43	0x02	PWM Output mode : 0x02 (DBTL mode) / 0x00(AD mode)
21	0x3C	0x64	Prescale Value 15W + 15W @PVDD20V / Load 6ohm
22	0x33	0x03	Soft Mute On Control
23	0x7E	0x03	Set 4-byte I2C Mode(Enable coefficient write for ch1/ch2)
24	0x00	0x107F2764	Set Bi-Quad filter coefficients BQ1 ~ BQ 16 
	0x01	0x11FF2764	
	0x02	0x107F2764	
	0x03	0x117F26AD	
	0x04	0x10FE5035	
	0x05	0x107FAAAC	
	0x06	0x11FC8820	
	0x07	0x10798F7E	
	0x08	0x117C8820	
	0x09	0x10F93A2A	
	0x0A	0x107CA59F	
	0x0B	0x11D8EE5B	
	0x0C	0x105DA082	
	0x0D	0x1158EE5B	
	0x0E	0x10DA4621	
	0x0F	0x1059D404	
	0x10	0x10DFBD44	
	0x11	0x0F64B509	
	0x12	0x105FBD44	
	0x13	0x0F985D10	
	0x14	0x1074AE71	
	0x15	0x11E53981	
	0x16	0x10613654	

0x17	0x11653981
0x18	0x10D5E4C4
0x19	0x107B6086
0x1A	0x11E75999
0x1B	0x10599250
0x1C	0x11675999
0x1D	0x10D4F2D6
0x1E	0x107ED010
0x1F	0x11FC937D
0x20	0x107AC0C6
0x21	0x117C937D
0x22	0x10F990D7
0x23	0x107F2CBA
0x24	0x11FEDF58
0x25	0x107E9840
0x26	0x117EDF58
0x27	0x10FDC4FA
0x28	0x110010DB
0x29	0x11FF9340
0x2A	0x107F0A70
0x2B	0x117F9340
0x2C	0x10FF2C26
0x2D	0x11000000
0x2E	0x20000000
0x2F	0x20000000
0x30	0x20000000
0x31	0x20000000
0x5C	0x11000000
0x5D	0x20000000
0x5E	0x20000000
0x5F	0x20000000
0x60	0x20000000
0x61	0x11000000
0x62	0x20000000
0x63	0x20000000
0x64	0x20000000
0x65	0x20000000
0x66	0x11000000
0x67	0x20000000

	0x68	0x20000000	
	0x69	0x20000000	
	0x6A	0x20000000	
	0x6B	0x11000000	
	0x6C	0x20000000	
	0x6D	0x20000000	
	0x6E	0x20000000	
	0x6F	0x20000000	
	0x70	0x11000000	
	0x71	0x20000000	
	0x72	0x20000000	
	0x73	0x20000000	
	0x74	0x20000000	
	0x75	0x11000000	
	0x76	0x20000000	
	0x77	0x20000000	
	0x78	0x20000000	
	0x79	0x20000000	
25	0x7E	0x08	Set APEQ Setting Enable - APEQ 4-byte I2C Mode
26	0x00	0x10000000	P0
	0x01	0x10000000	
	0x02	0x10000000	
	0x03	0x10000000	
	0x04	0x10000000	
	0x05	0x10000000	
	0x06	0x11000000	P1
	0x07	0x11000000	
	0x08	0x11000000	
	0x09	0x11000000	
	0x0A	0x11000000	
	0x0B	0x11000000	
	0x0C	0x11000000	P2
	0x0D	0x11000000	
	0x0E	0x11000000	
	0x0F	0x11000000	
	0x10	0x11000000	
	0x11	0x11000000	
	0x12	0x20000000	P3
	0x13	0x20000000	

	0x14	0x20000000	Threshold
	0x15	0x20000000	
	0x16	0x20000000	
	0x17	0x20000000	
	0x1F	0x11000000	
	0x20	0x11000000	
	0x21	0x11000000	
	0x22	0x11000000	
	0x23	0x11000000	
	0x24	0x11000000	
27	0x7E	0x00	Set 1-byte I2C Mode(Disable coefficient write for ch1/ch2)
28	0x33	0x00	Soft Mute Off Control
29	0x19	0x00	APEQ Path Option
30	0x1A	0x10	APEQ1 attack time = 4ms / release time = 1sec
31	0x1B	0x10	APEQ2 attack time = 4ms / release time = 1sec
32	0x1C	0x10	APEQ3 attack time = 4ms / release time = 1sec
33	0x1D	0x10	APEQ4 attack time = 4ms / release time = 1sec
34	0x1E	0x10	APEQ5 attack time = 4ms / release time = 1sec
35	0x1F	0x10	APEQ6 attack time = 4ms / release time = 1sec
36	0x0E	0x00	CH1_BQ1~BQ3 Enable
37	0x0F	0x00	CH2_BQ1~BQ3 Enable
38	0x10	0x00	CH1_BQ4~BQ6 Enable
39	0x11	0x00	CH2_BQ4~BQ6 Enable
40	0x12	0x00	CH1_BQ7~BQ10 Enable
41	0x13	0x00	CH2_BQ7~BQ10 Enable
42	0x14	0x00	CH1_BQ11~BQ12 Enable
43	0x15	0x00	CH2_BQ11~BQ12 Enable
44	0x68	0x60	Phase 90° : 0x60(DBTL Mode), Phase 0° : 0x00(PBTL/AD mode)
45	0x4A	0x00	PWM Soft start Disable
46	0x24	0x00	RS DRC Enable
47	0x25	0x01	Vrms Period for Low-Band
48	0x4D	0x01	Vrms Period for High-Band
49	0x4E	0x01	Vrms Period for Sub-Band
50	0x4F	0x01	Vrms Period for Post-Band
51	0x2D	0x0A	Threshold Table Mapping
52	0x07	0x00	Vrms DRC Release Filter On
53	0x0E	0x00	BQ1 Loudness filter Enable : 0x0E(1:0) = b10, 0x0F(1:0) = b10 Disable : 0x0E(1:0) = b00, 0x0F(1:0) = b00

54	0x0F	0x00	
55	0x31	0x00	ReBASS Parameter Selection (Volume 0~4: 0x00 ~0x04, Gain 0~4 : 0x05~0x09, Slope 0~3 : 0x0A~0x0D)
56	0x32	0x00	ReBASS Parameter Value
57	0x08	0x00	TV Volume : 0 ~100
58	0x3D	0x00	WCK Synchronizing Control
59	0x0C	0xFF	Master volume Control
60	0x16	0x00	Master Fine Volume : 0 dB

Sound Off Sequence

No	Register	Setting Value	Description
1	0x33	0x03	Softmute (decrease)
2	0x34	0x03	Channel n PWM switching OFF
3	0x35	0x06	Reset the auto PWM_MASK restore counter to 0

Sound On Sequence

No	Register	Setting Value	Description
1	0x35	0x04	Reset the auto PWM_MASK restore counter to 0
2	0x34	0x00	Channel n PWM switching ON
3	0x33	0x00	Softmute (Increase)

Table 2. Initialization code

4. Description DRC & Prescaler

4.1. DRC

4.1.1. Definition

Dynamic Range Compression (DRC) in WA20-6829B limits the output level not to exceed the threshold level by reducing the signal gain.

4.1.2. Threshold

DRC in WA20-6829B does not perform expanding function, and 'threshold' is defined as the level where DRC starts to work; in other words, DRC limit the output level that exceeds the predefined 'threshold' level.

4.1.3. Attack & Release Time

'Attack time' is defined as a time required reducing the gain for the input signal down to the threshold level as shown in Figure 15.

Whereas, 'release time' is defined as a time required restoring the reduced gain to the original level when the signal level goes below threshold.

Considerations for gain change

Attack time: if too short attack time is applied, pop noise can be occurred. On the other hand, too long attack time can result in clipping of the output when the input level goes high in a short period.

Release time: if too long release time is applied, a small signal input can be heard too quiet after the large gain reduction is applied. On the contrary, if too short release time is used, pumping effect can be caused, where the signal level is fluctuated by periodic gain reduction and restoration.

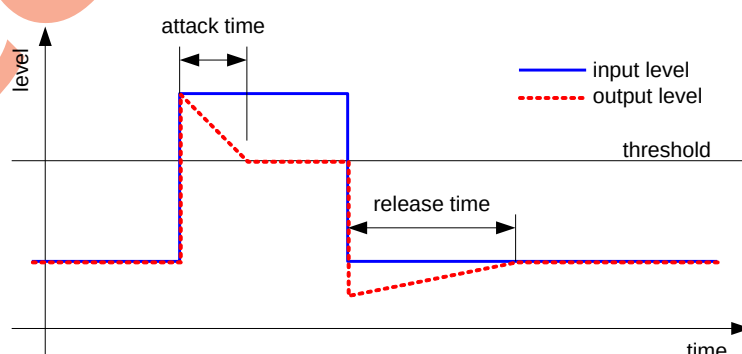


Figure 15. Attack time, release time

4.1.4. Gain curve

Figure 16 is an example of various gains according to the input level. When the input level is less than -12dB, the gain is 0dB, which means the input signal is directly bypassed to the output. If the input is above -12dB, the input is compressed. When the input exceeds +12dB, the output level is limited to 0dB, and the function is a limiter, which confines the output level to 0dB regardless of the input level. Figure 16(b) is the gain curve for the input versus output relation of Figure 16(a).

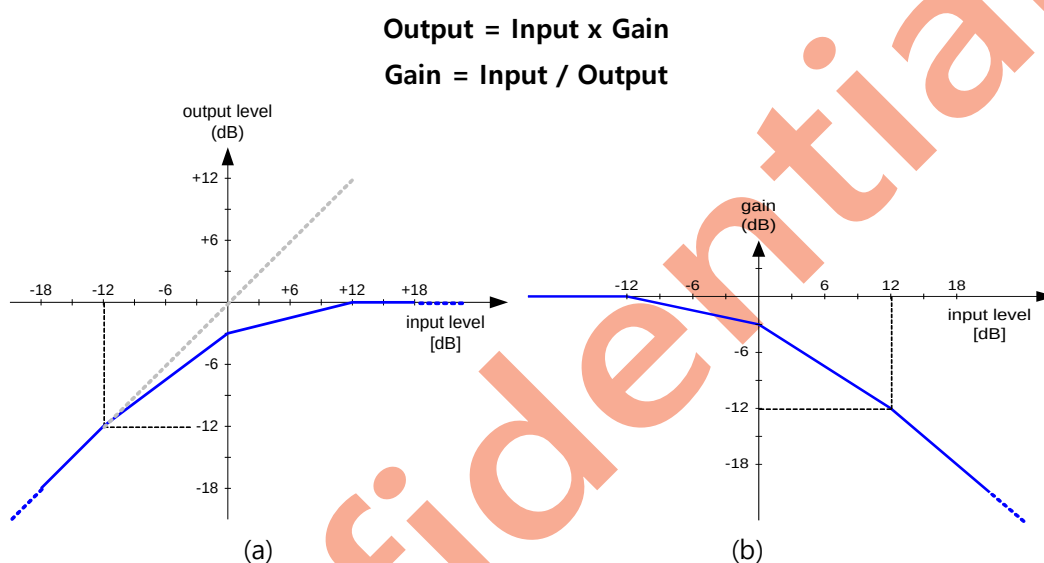


Figure 16. Compression curve, gain curve

4.1.5. 1Band DRC structure

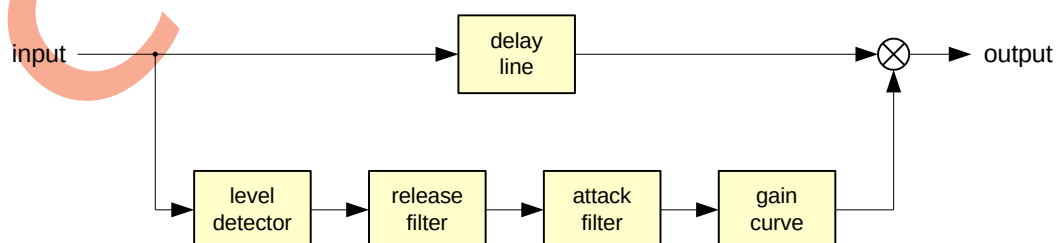


Figure 17. DRC block diagram

Figure 17 shows the whole DRC structure. The level detector tracks the envelope of the input signal. If attack and release time is 0, the gain curve can be instantly applied to the signal.

However, there is time delay of attack and release time, and attack and release filter is used. The gain is obtained in the end, and it is applied to the input signal to produce DRC output.

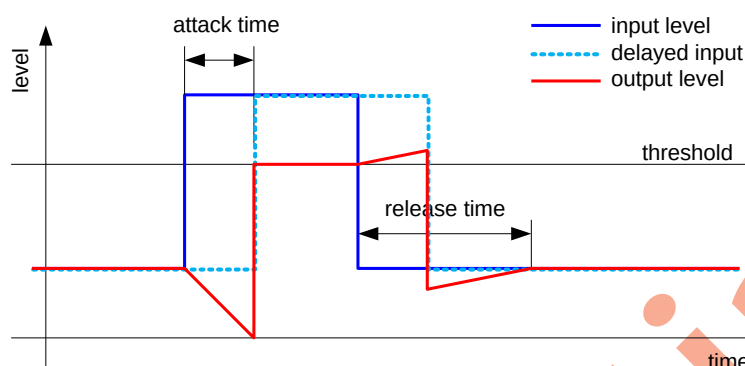


Figure 18. DRC attack, release using delay line

Delay line can relieve early overshooting of the output when the signal is being attacked by DRC. If the delay line has the same delay time of the attack time, overshooting of the output can be prevented as shown in Figure 18. Yet, such delay time requires quite a large memory size, so there exists a tradeoff.

4.1.6. Two Band DRC structure

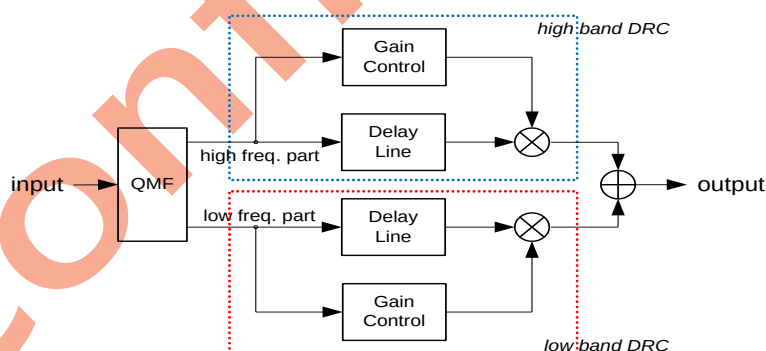


Figure 19. Band DRC structure

Figure 18 represents a two band DRC that can handle low and high frequency bands separately. QMF divides the input signal into two bands, and the DRC handles each band independently. After DRC processing, each band is merged to produce the output. Each DRC has the same structure of the one band DRC in Figure 19.

4.1.7. Three Band DRC structure

Three Band DRC add sub band to control sub band below 200Hz, while the structure for the other 2 band is the same.

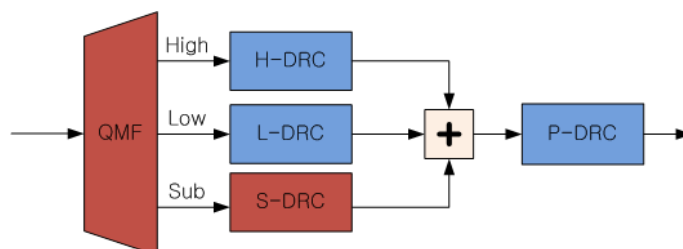


Figure 20. 3 Band DRC structure

The input signal is divided into three band by the QMF (quadrature mirror filter bank), and each band is processed independently. Finally, each output of three bands is merged into the final output. The whole structure of three band DRC is illustrated in Figure 20.

4.1.8. QMF(Quadrature Mirror Filter)

QMF is composed of analysis filter banks, which divide the signal, and synthesis filter banks, which put the signals together. If no processing is applied between the analysis filter banks and synthesis filter banks, QMF reconstructs the original signal perfectly except for the time delay (perfect reconstruction filter bank). This QMF can be designed using FIR or IIR filter. Needless to say, a cross-over frequency that divides high and low frequency bands can be selected.

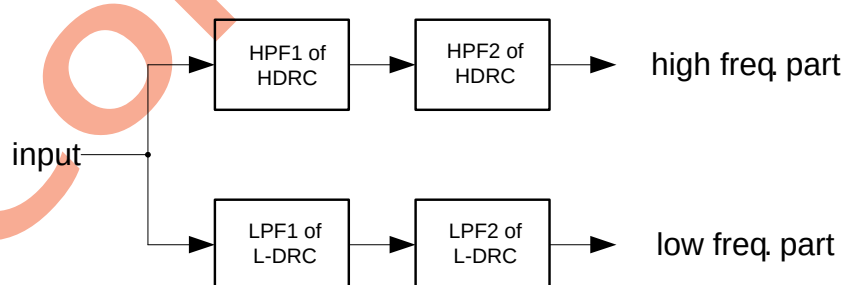


Figure 21. QMF filter structure of enhanced DRC

4.1.9. DRC Setting sequence

■ Register setting

The address range for DRC registers is 0x20 ~ 0x2C. These are for Threshold, Attack Time, Release Time, Delay line length, Enable/Disable registers of 3 band DRC.

■ Initialization

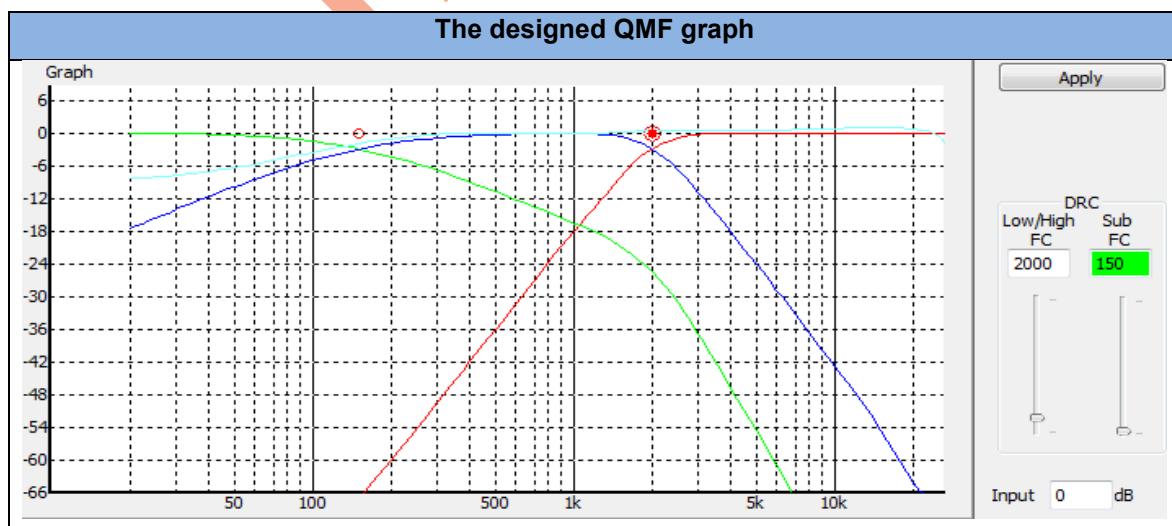
When initializing the amplifier, set Coefficient, Threshold, Attack time, Release time, DRC On/Off. The following table is an example sequence.

No	Register	Setting Value	Description
1	0x7E	0x03	Set 4-byte I2C Mode (Enable coefficient write for ch1/ch2)
2	0x32	0x0C7BF3C4	DRC QMF_BQ1
	0x33	0x0C7BF3C4	
	0x34	0x20000000	
	0x35	0x10608188	
	0x36	0x20000000	
	0x37	0x0903947F	DRC QMF_BQ2
	0x38	0x0A03947F	
	0x39	0x0903947F	
	0x3A	0x116E42A2	
	0x3B	0x10E0A1E8	
	0x3C	0x107040C4	DRC QMF_BQ3
	0x3D	0x10F040C4	
	0x3E	0x20000000	
	0x3F	0x10608188	
	0x40	0x20000000	
	0x41	0x106F49CB	DRC QMF_BQ4
	0x42	0x11EF49CB	
	0x43	0x106F49CB	
	0x44	0x116E42A2	
	0x45	0x10E0A1E8	
	0x46	0x092010AB	DRC QMF_BQ5
	0x47	0x092010AB	
	0x48	0x20000000	
	0x49	0x107D7FBD	
	0x4A	0x20000000	
	0x4B	0x11000000	DRC QMF_BQ6
	0x4C	0x20000000	

	0x4D	0x20000000	
	0x4E	0x20000000	
	0x4F	0x20000000	
3	0x7E	0x00	Set 1-byte I2C Mode (Disable coefficient write for ch1/ch2)
4	0x20	0xA8	low band DRC threshold = 0dB
5	0x21	0x10	low band DRC attack time = 4ms / release time = 1sec
6	0x22	0xA8	high band DRC threshold = 0dB
7	0x23	0x10	high band DRC attack time = 4ms / release time = 1sec
8	0x26	0x9E	Post DRC threshold = 1dB
9	0x27	0x10	Post DRC attack time = 4ms / release time = 1sec
10	0x2A	0xA8	sub band DRC threshold = 0dB
11	0x2B	0x11	sub band DRC attack time = 8ms / release time = 1sec
12	0x29	0x11	2Band DRC mode enable
13	0x2C	0x01	Sub band mode enable
14	0x24	0x00	RS DRC Enable
15	0x25	0x01	Vrms Period for Low-Band
16	0x4D	0x01	Vrms Period for High-Band
17	0x4E	0x01	Vrms Period for Sub-Band
18	0x4F	0x01	Vrms Period for Post-Band
19	0x2D	0x0A	Threshold Table Mapping
20	0x07	0x00	Vrms DRC Release Filter On

Table 3. DRC QMF Initialization code

4.1.10. Designed QMF Graph



4.1.11 Setting sequence

1) DRC select

Addr 0x29 (1Band or 2Band DRC mode select)

Addr 0x2C (Sub Band DRC Mode select)

2) DRC Enable/Disable

Addr 0x20 (1Band DRC Enable/Disable)

Addr 0x22 (2Band DRC Enable/Disable)

Addr 0x2A (Sub Band DRC Enable/Disable)

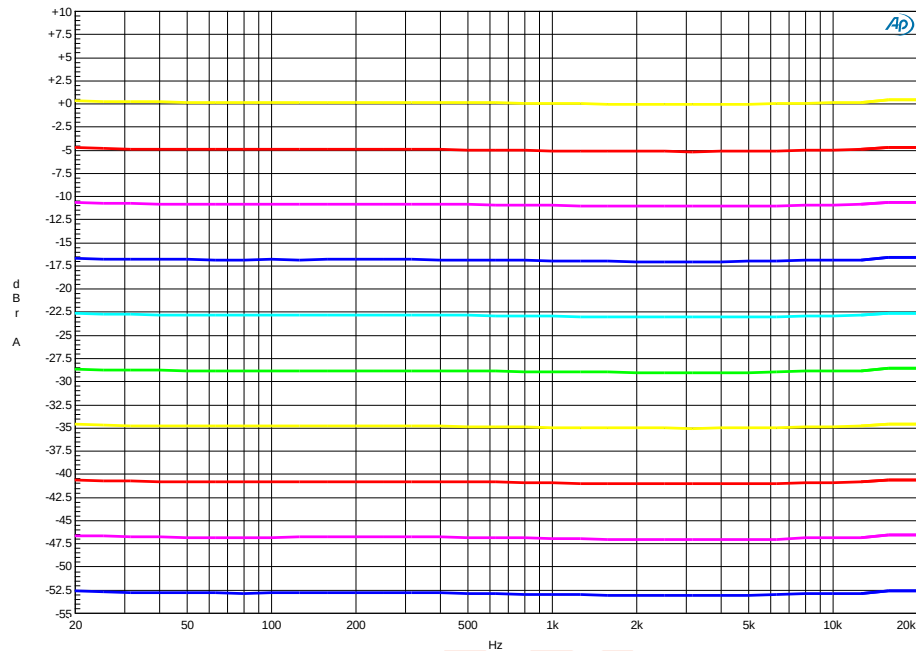
3) Coefficient Register (Address 0x32 ~ 0x4F)

3B' DRC Coefficient mode register	0x32 ~ 0x36	0x37 ~ 0x3B	0x3C ~ 0x40	0x41 ~ 0x45	0x46 ~ 0x4A	0x4B ~ 0x4F
When System Address 0x7E = 0x03	LPF1 of L-DRC	LPF2 of L-DRC	HPF1 of H-DRC	HPF2 of H-DRC	SPF1 of S-DRC	SPF2 of S-DRC

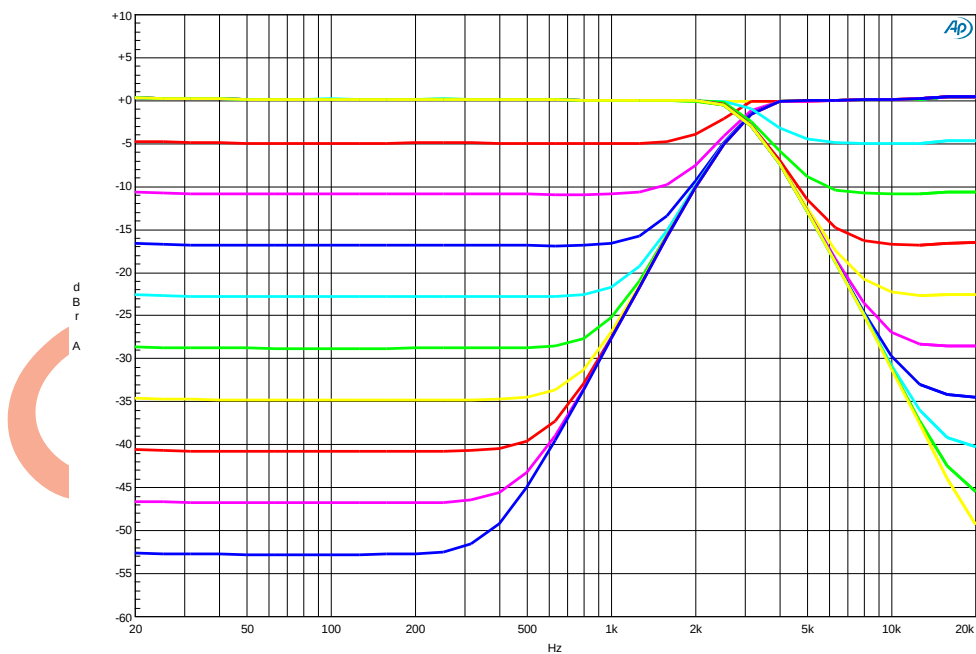
Table 4. Coefficient Register map

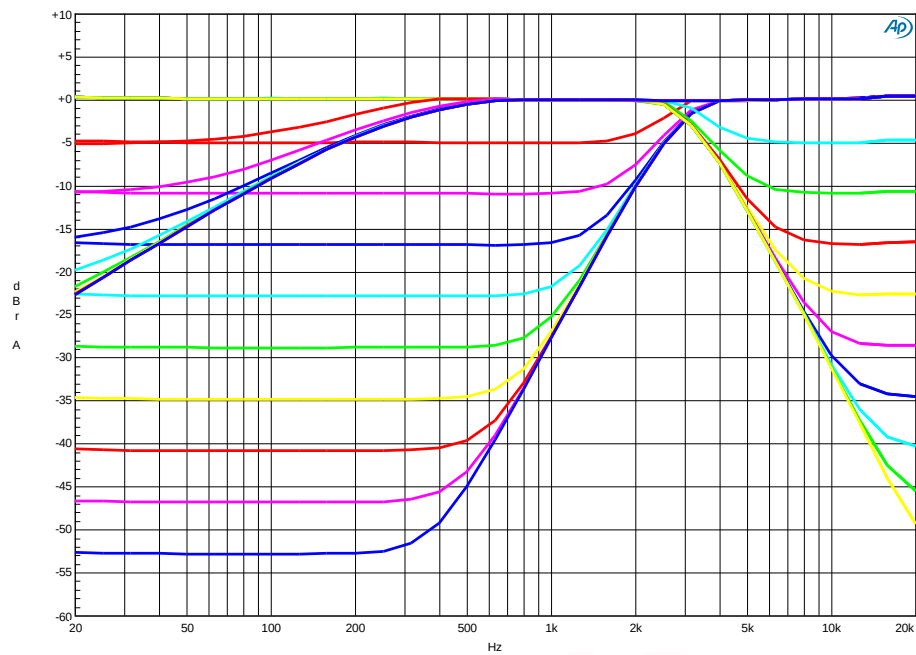
4) Measurement of 3Band DRC

A. 1 Band DRC(0,-6,-12,-18,-24,-30,-36,-42,-48,-54dB)



B. 2 Band DRC(0,-6,-12,-18,-24,-30,-36,-42,-48,-54dB)



C. 3 Band DRC(0,-6,-12,-18,-24,-30,-36,-42,-48,-54dB)

4.2 Pre-scaler

4.2.1 Definition

Prescaler limits the maximum width of PWM pulse according to the preset level. Adjusting the Prescaler value can effect as changing PVDD voltage to manipulate maximum power output under the fixed PVDD supply. Therefore, the Prescaler value is useful when variant models of different maximum power outputs are developed with the same design platform.

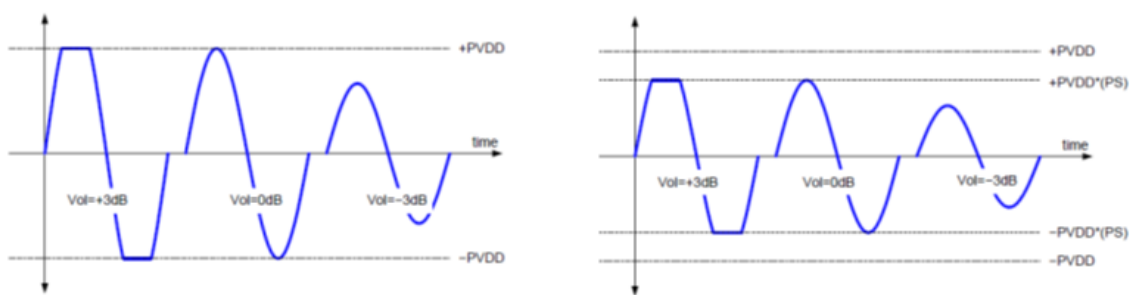


Figure 22. Pre-scaling

✓ How to calculate output power using Prescaler

1) Prescaler (PS) vs. Output Power and driven voltage.(PVDD)

2) Power = $(I_{rms}^2) \cdot R$

$$= (I_{peak} \cdot 0.707)^2 \cdot R$$

$$= (((PVDD \cdot (PS/127)) / (Z_{spk} + R_{loss})) \cdot 0.707)^2 \cdot R$$

3) Note :

Z_{spk} : Speaker Impedance

R_{loss} : Parasitic resistance in output line of audio.

5. ReBASS

5.1 ReBASS Control

ReBASS enriches the sound of low frequency of audio signal without clipping and distortion. ReBASS is to compensate the characteristics of human loudness perception. For instance, when the volume level is low, the gain of the low frequency band is boosted. On the other hand, when the volume level closes to the maximum, the gain can be minimized to avoid sound clipping. All these scenarios can be set by user by selecting up to four inflection points in the volume-gain curve. While applying the adaptive gain control according to the volume, enhanced bass sound is to be reproduced without sound clipping at the high volume level.

The gain boosting depending on volume level can be changed by rewriting the REBASS parameter table which consists of 5 volume levels, 5 gain levels, and 4 slopes. In order to access the parameter table, two registers (0x31 and 0x32) are used. The first register (0x31) contains the index of the corresponding parameter, and the second register (0x32) contains the value of the indexed parameter. ReBASS calculates adaptive gains based on the parameter table whenever the volume level is changed.

5.2 ReBASS Structure

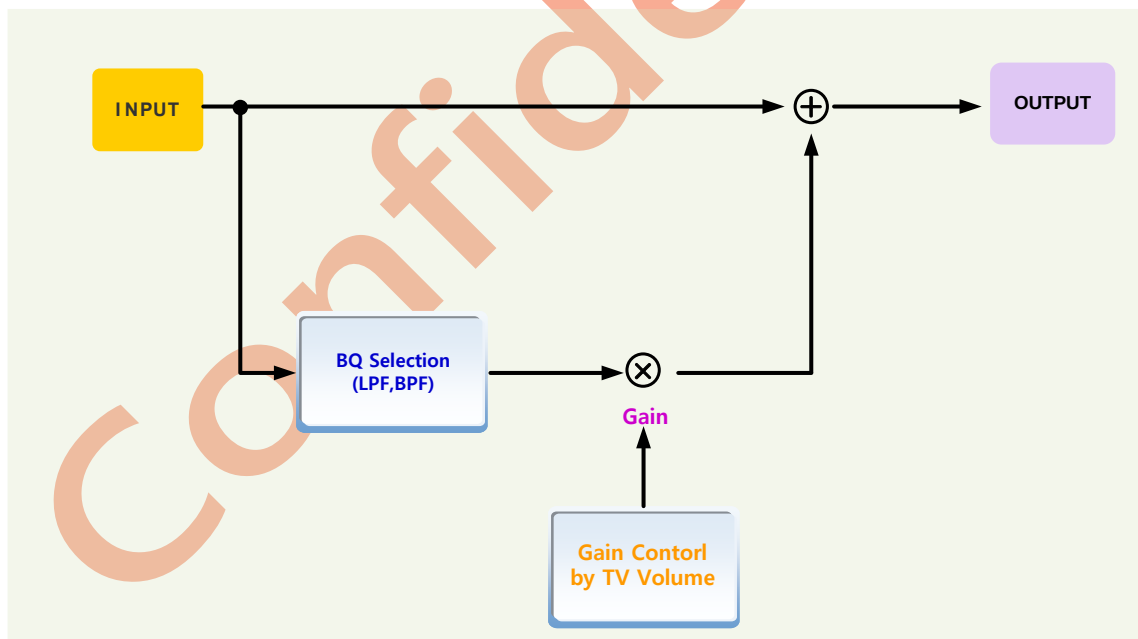
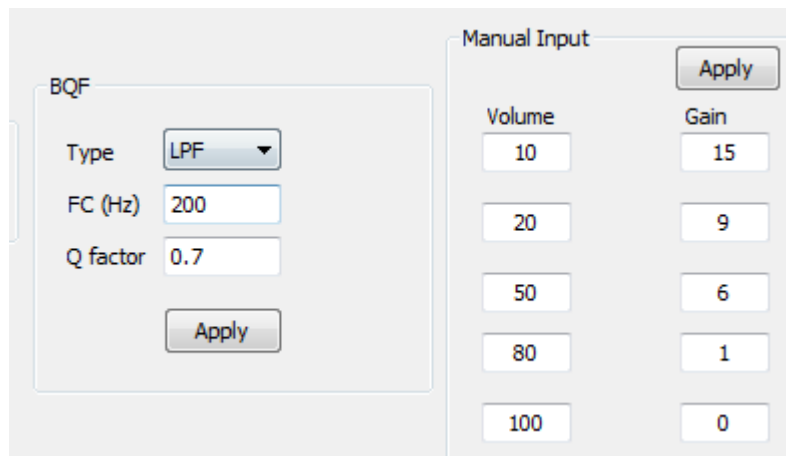


Figure 23. ReBASS Structure

5.3 ReBASS Setting

5.3.1 ReBASS Parameter Setting Value



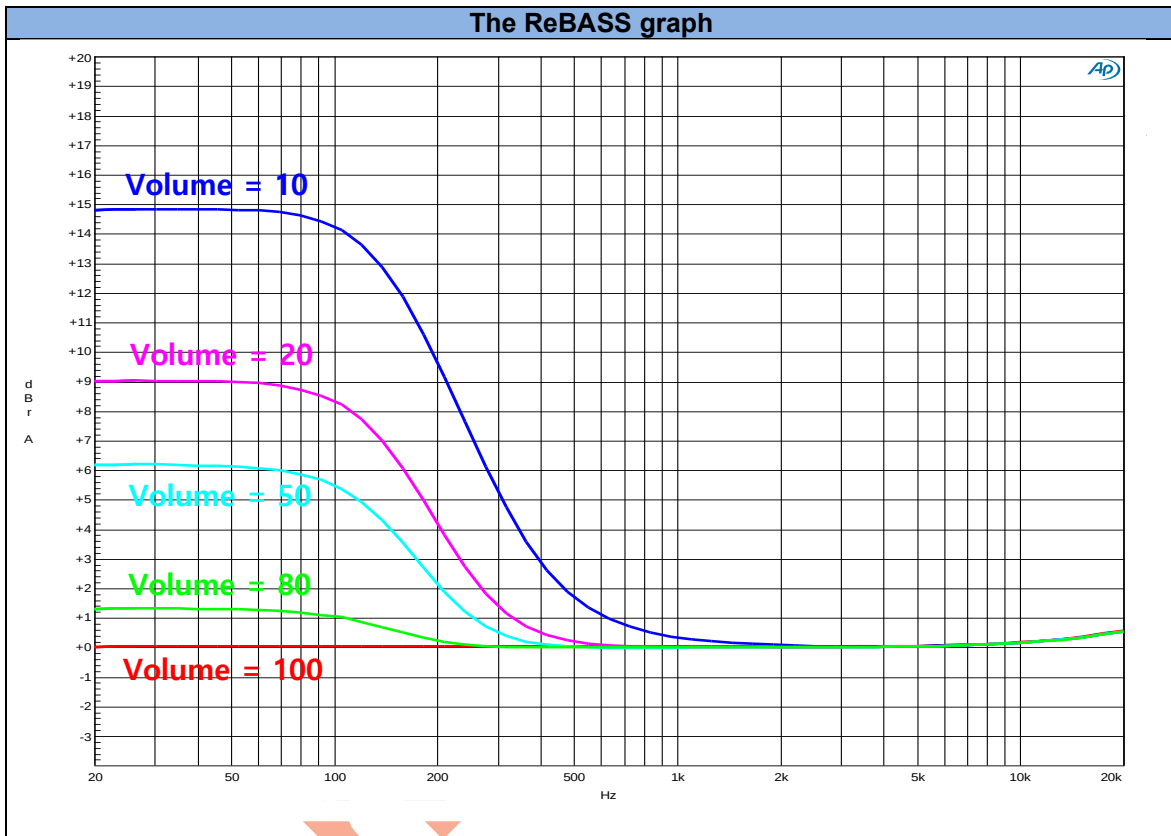
Manual Input	
Volume	Gain
10	15
20	9
50	6
80	1
100	0

5.3.2 ReBASS Setting example

No	Register	Setting Value	Description
1	0x0E	0x02	BQ1 Loudness filter Enable : 0x0E(1:0) = b10, 0x0F(1:0) = b10 Disable : 0x0E(1:0) = b00, 0x0F(1:0) = b00
2	0x0F	0x02	
3	0x31	0x00	Volume0
	0x32	0x0A	Vol : 10
	0x31	0x01	Volume1
	0x32	0x14	Vol : 20
	0x31	0x02	Volume2
	0x32	0x32	Vol : 50
	0x31	0x03	Volume3
	0x32	0x50	Vol : 80
	0x31	0x04	Volume4
	0x32	0x64	Vol : 100
	0x31	0x05	Gain0 (dB)
	0x32	0x0F	15dB
	0x31	0x06	Gain1 (dB)
	0x32	0x09	9dB
	0x31	0x07	Gain2 (dB)
	0x32	0x06	6dB
	0x31	0x08	Gain3 (dB)
	0x32	0x01	1dB
	0x31	0x09	Gain4 (dB)
	0x32	0x00	0dB
	0x31	0x0A	$Slope0 = (Gain1 - Gain0)/(Vol1 - Vol0)$
	0x32	0xDA	Slope0 : 0xDA
	0x31	0x0B	$Slope1 = (Gain2 - Gain1)/(Vol2 - Vol1)$
	0x32	0xFA	Slope1 : 0xFA
	0x31	0x0C	$Slope2 = (Gain3 - Gain2)/(Vol3 - Vol2)$
	0x32	0xF6	Slope2 : 0xF6
	0x31	0x0D	$Slope3 = (Gain4 - Gain3)/(Vol4 - Vol3)$
	0x32	0xFD	Slope3 : 0xFD
4	0x7E	0x03	4-byte I2C Mode
5	0x33	0x03	Soft Mute On Control
6	0x00	0x0825CE7C	Filter = LPF Fc=200Hz Q factor=0.7
	0x01	0x0248AA9B	
	0x02	0x08A2ABD1	
	0x03	0x117E3490	

	0x04	0x10FC6F66	
7	0x7E	0x00	1-byte I2C Mode
8	0x33	0x00	Soft Mute Off Control

5.3.3 ReBASS Graph (Filter Type : LPF, FC : 200Hz, Q : 0.7)



6. Hardware

6.1. Recommended circuit

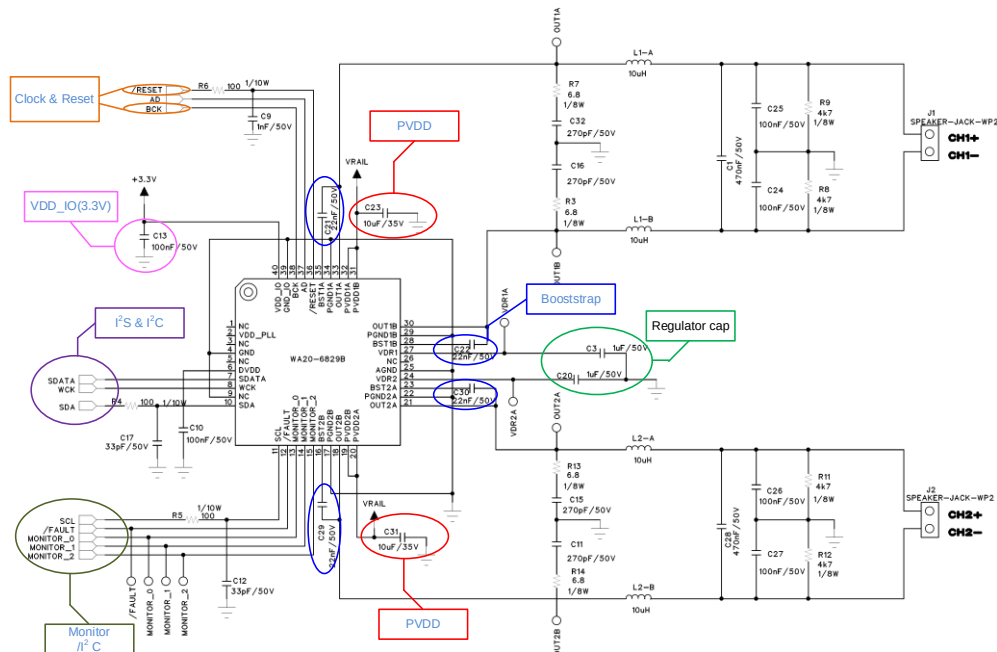


Figure 24. Recommend circuit

6.2. Power sequence

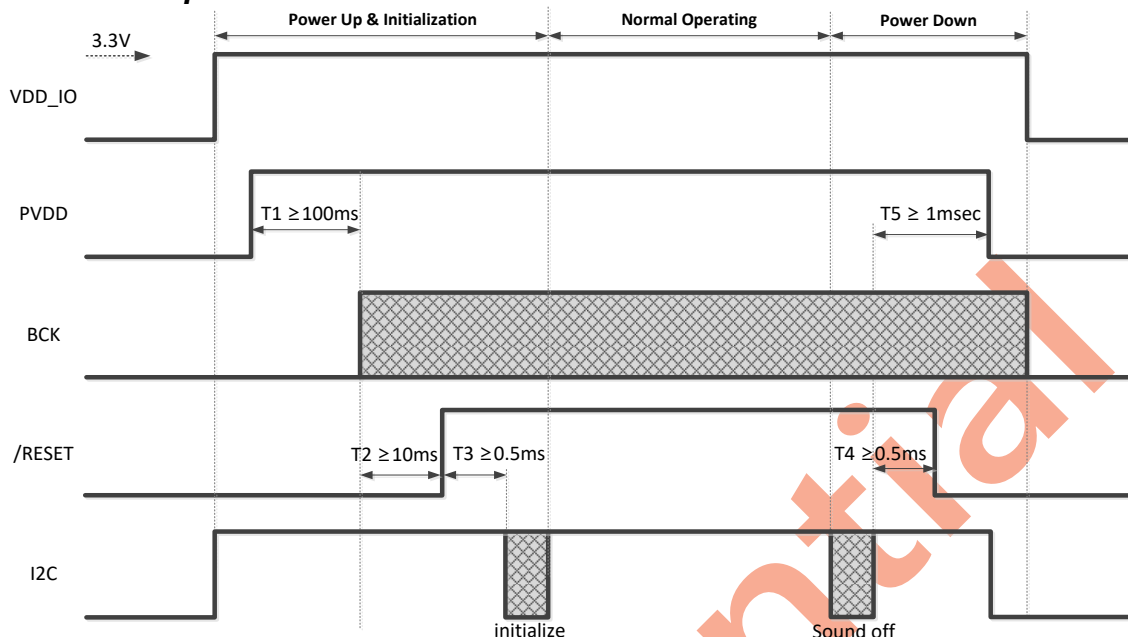


Figure 25. Power sequence

✓ Power-Up & Initialization Sequence

- 1) Ramp up VDD_IO to at least 3.3V.
- 2) Ramp up PVDD (7~28V).
- 3) Drive BCLK signal at least 100ms after PVDD ($T1 \geq 100\text{msec}$).
- 4) At least 10ms after BCLK, Drive /RESET = High ($T2 \geq 10\text{msec}$).
- 5) Wait for at least 0.5msec for I²C communication ($T3 \geq 0.5\text{msec}$) and keep the status.
- 6) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

✓ Power-Down Sequence

- 1) When both DC and AC power are off, make sure to execute sound off sequence.
- 2) Switch /RESET to Low at least 0.5 msec after sound off sequence ($T4 \geq 0.5\text{msec}$).
- 3) Ramp down PVDD at least 0.5 msec after sound off sequence ($T5 \geq 1\text{msec}$).
- 4) After I²C is Low, ramp down VDD_IO.

6.3. Output power for PVDD

- ✓ Max Output by PVDD @ 8ohm , 6ohm
- ✓ Test Condition
 - 1) PCB : 95mm X95mm
 - 2) Input: sinwave 1kHz 0dBfs
 - 3) Volume setting: 0dB Fs

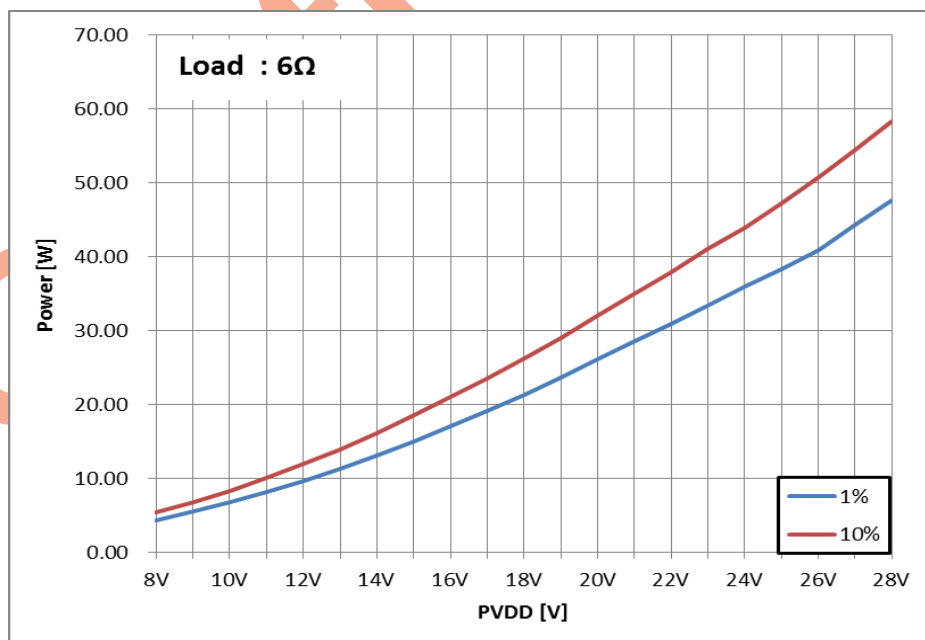
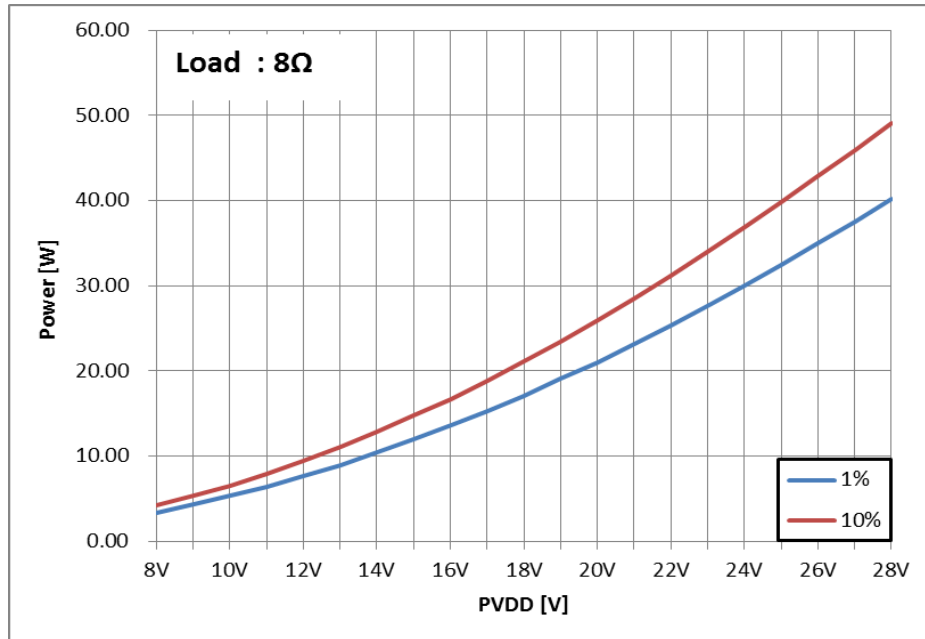


Table 5. WA20-6829B output power vs PVDD

6.4. Output Filter-design

The LC filter design for WA20-6829B is similar to that for general class D or other full digital amp. For instance, an LC filter stage of 22uH Inductor and 470nF Capacitor shows the cut off frequency of 50KHz.

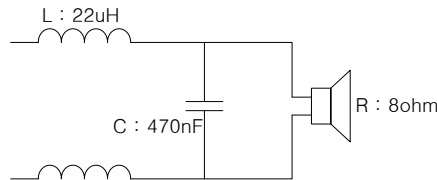


Figure 24. LC Filter

$$Q \text{ Factor} = R * \sqrt{\frac{C}{2 * L}}$$

Formula <1> Q-Factor

$$\text{Cut Off Frequency} = \frac{1}{(2 * \pi * \sqrt{2 * L * C})}$$

Formula <2> Cut Off Frequency

L value	C value	R value	Q factor	Fc
22uH	470nF	8 ohm	0.826	35kHz
22uH	470nF	6 ohm	0.620	35kHz
22uH	470nF	4 ohm	0.413	35kHz
15uH	470nF	8 ohm	0.500	42.4kHz
15uH	470nF	6 ohm	0.751	42.4kHz
15uH	470nF	4 ohm	1.001	42.4kHz
10uH	470nF	8 ohm	1.226	51.9kHz
10uH	470nF	6 ohm	0.919	51.9kHz
10uH	470nF	4 ohm	0.613	51.9kHz

Table 6. The result of LC Filter

RC Filter in Reset and Fault pin

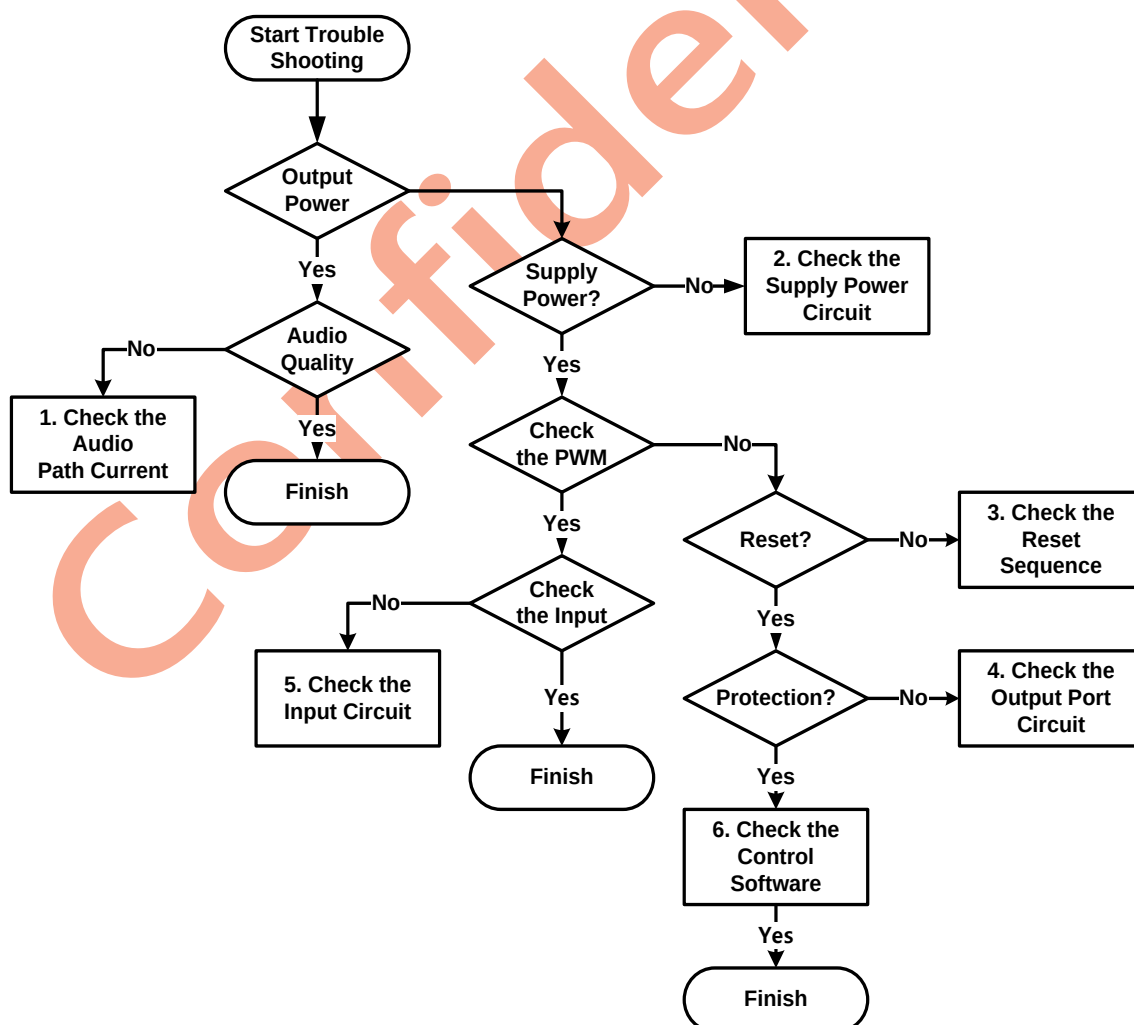
To prevent glitch noise from other source, an RC filter is recommended for Reset pin and Fault pin. The recommended value is 100ohm and 1nF.

$$\text{Cut Off Frequency} = \frac{1}{2 * \pi * R * C}$$

Formula <3> Cut Off Frequency of RC filter

7. Trouble shooting guide

7.1. Check Flow



7.2. Checking circuit for sound quality

Check I2S format

- 1) Check BCK and WCK of the I2S signal.

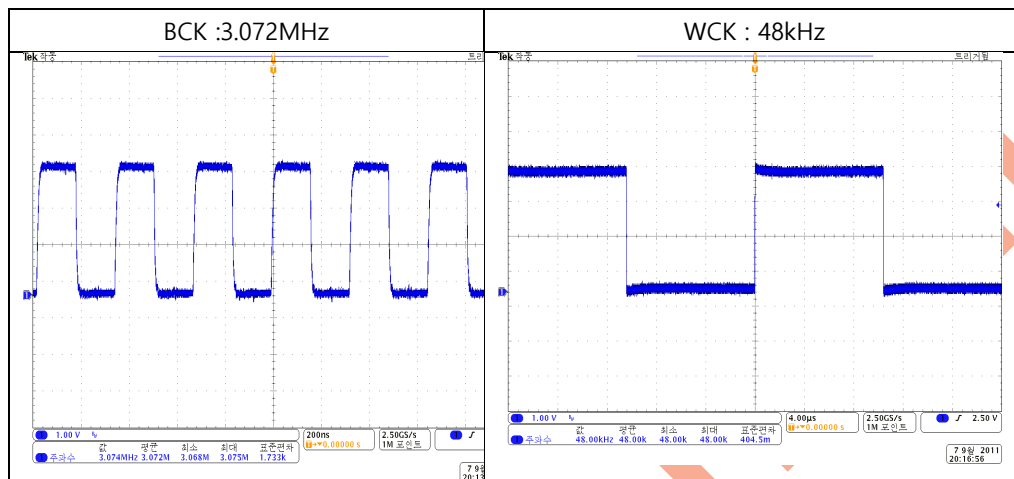


Figure 25. I2S (BCK, WCK)

- 2) Check WCK and SDATA signal using Oscilloscope and verify that the format is coherent to the CP setting. (e.g. Audio Data Format: I2S, Fs: 48 kHz)

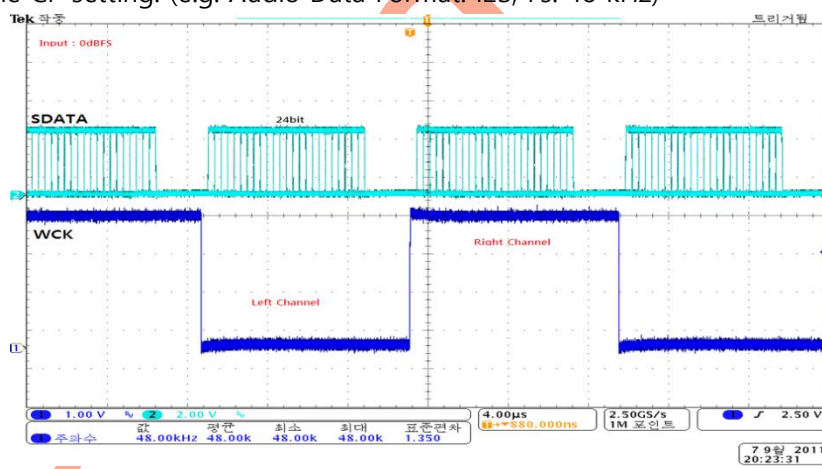


Figure 26. I2S (SDATA, WCK)

Check I2S Data

- 1) Apply 'softmute' using the CP setting, and check whether the noise disappears.
- 2) Set the gain of Mixer for L/R channel as -150dB and check whether the noise disappears.

7.3. Checking power circuit

- 1) Check the voltage of PVDD, VDDIO, VDD_PLL, AVDD_PLL.

☞ VDD_IO: 3.3V, AVDD_PLL & DVDD_PLL: 1.2V

7.4. Checking output

- 1) Check whether the PWM pulse output is generated.
 - If the PWM pulse does not appear, check the output load impedance (e.g. whether the load is near "0 ohm" or short-circuit).
 - Check whether the VDR voltage $\approx 5.1V$.
- 2) Inspect whether there is damage in the speaker or inductor.
- 3) Check the speaker impedance. If the speaker impedance is too low, current protection can occur.
- 4) Check excessive ripple of the PWM output.
- 5) After the LC filter stage, check whether excessive magnitude of carrier frequency is measured.
- 6) Check whether proper value of inductors and capacitors are chosen for the LC Filter.

7.5. Checking Software (Control Program)

- 1) Check the setting of master volume, channel volume, mixer gain, softmute registers.
- 2) Check whether the level of I2S Data is large enough to output a signal.
- 3) Investigate the I2C line using an oscilloscope so that SCL and SDA of I2C are normal and operational. Check the proper ACK is occurring.

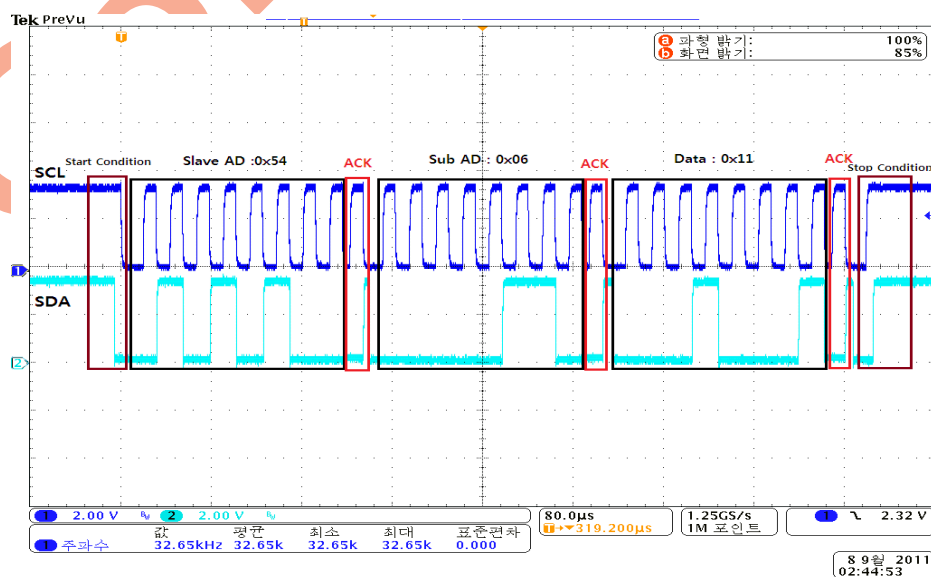


Figure 27. I2C Communication

7.6. Checking input

- 1) Check whether SDATA, WCK, and BCK of I2S are properly applied to the input.
- 2) Check whether MCLK is normal.

Confidential